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1 April 1981 through 31 March 1982

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J. D. Meindl, Director
Stanford Electronics Laboratories
Stanford University   Stanford, California
(415) 497-1013

CONTENTS

Document describes

in the areas of

ILLUSTRATIONS

ILLUSTRATIONS (Cont)

I. RESEARCH PROGRAM

A. Very Large Scale Integration

1. Properties of Materials: Application of Channeling Radiation to a Study of the Properties of Materials

Principal Investigator: R. H. Pantell

Scientific Objective

The objective of this project is to study the properties of materials in which channeling occurs by means of channeling radiation.

Progress

The existence of radiation from channeled relativistic charged particles has been predicted [1,2] and we have reported the first observation of channeling radiation [3,4]. After our initial observation of the spectral lines associated with channeling radiation, many experimental and theoretical investigations have followed [5,6,7]; particle energies ranged from 1.5 MeV to 10 GeV, and diamond [8,9], Si [3,4,5], Ge [10], Au [11], LiF [12], and Ni [13] crystals were used in the experiments.

To date, only cubic-structure (diamond and simple cubic) crystals have been used. We are preparing other crystals such as MgF_2 with its tetragonal structure and CaF_2 with its fluorite structure.

We have measured and compared channeling radiation in diamond with and without the presence of platelets. Platelets are clusters of nitrogen impurities in the form of thin disks present in many natural diamonds. Because they are a single atomic layer thick, the plane of the disks is parallel to the {100} planes of the crystal. This type of defect is of particular interest to channeling radiation because its effects depend on crystal orientation. For {100} planes, the platelets distort the existing planes and become a scattering center. For {110} and {111} planes, the platelets appear as a stacking fault [14] which is far less inhibiting to channeling; indeed, for the {111} planes, there is only a 24 percent reduction in the intensity of channeling radiation in diamond with platelets and over a 30 percent reduction in linewidth

which is contrary to what would be expected from the introduction of a defect. The most likely explanation is that the stacking fault preferentially removes the population from the eigenstates that contribute the most to line broadening. We are studying this effect.

We are also planning to investigate channeling radiation at a low temperature around 80 K. Because atomic thermal vibrations are the primary coherence-limiting effect, this should result in line narrowing. Our calculation (in good agreement with experimental results at room temperature) indicates that the linewidth of channeling radiation in silicon at 80 K would be approximately half of that at room temperature, and this type of line narrowing correspondingly increases peak amplitude. Channeling radiation will be a more useful source of soft and hard X-rays if the linewidth can be narrowed and peak intensity increased.

a.   Channeling Radiation from Relativistic Positrons in LiF

We reported the first observation of channeling radiation from a binary crystal [12]. For both {100} and {110} planes, all planes contain both Li and F atoms, and the potential function is close to harmonic which yields almost equally spaced eigenvalues and, therefore, a single spectral line. The {111} planes, however, contain separate atoms of Li and F so that the potential function is much more complicated. Figure A.1a shows the potential function and energy levels of LiF {111} planes for 54 MeV positrons. The channeling radiation spectrum of a 25 µm LiF crystal is plotted in Fig. A.1b plus the theoretical predictions based on the potential in Fig. A.1a. The height of these lines indicates the relative intensities of the transitions, and a uniform population at each level was assumed. These calculations are in good agreement with the experimental data.

Figure A.2 shows the {100} channeling-radiation spectrum over a wider energy range. The peak in the spectrum at 120 keV results from $\Delta n = 3$ transitions between the bound states, as we have seen in electrons channeled in silicon [5]. The intensity of these transitions

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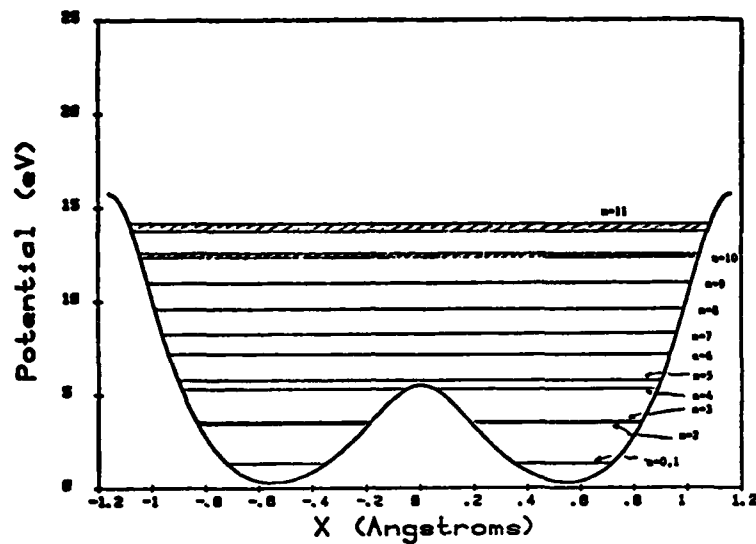
a.   Calculated interplanar potentials
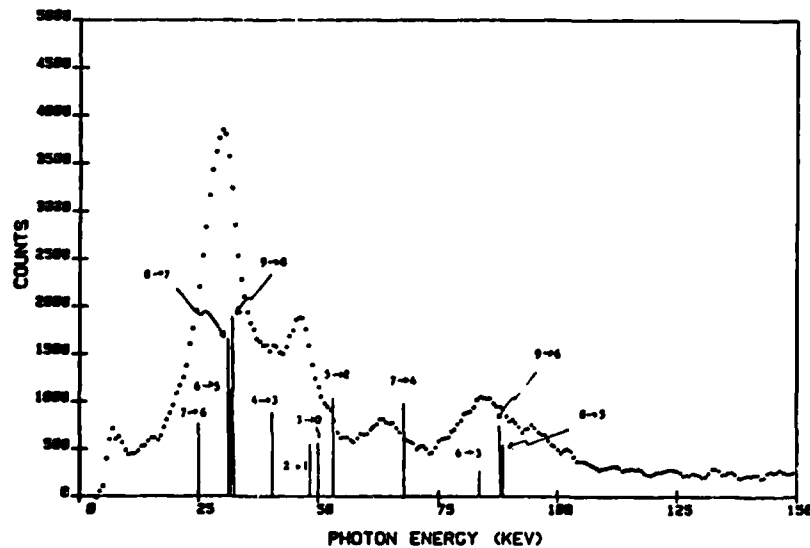
b.   Measured background-corrected radiation spectrum
     from 54 MeV positrons

Fig. A.1.   CHANNELING RADIATION IN THE {111} PLANE IN
     LiF.

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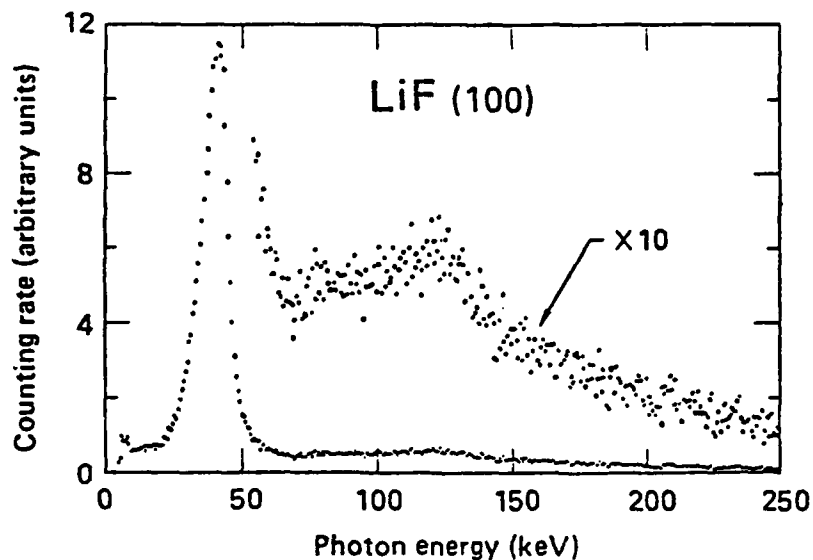
Fig. A.2. MEASURED BACKGROUND-CORRECTED RADIATION
SPECTRUM FROM 54 MeV POSITRONS CHANNELED ALONG
THE {100} PLANE IN LiF. The $\Delta n = 3$ transitions
can be seen.

is proportional to the anharmonicity of the potential [16]; in a harmonic potential, the matrix elements vanish.

The dechanneling length for 54.5 MeV positrons along the {100} plane in LiF can be estimated by comparing the channeling-radiation intensities in crystals of different thicknesses. The measured ratios of the counting rates for channeling radiation and for bremsstrahlung (as approximated by placing the LiF crystal in a random orientation with respect to the incident-beam direction), both integrated over the photon energy range from 24 to 57 keV, were 6.2, 4.0, and 3.7 for crystal thicknesses of 25, 125, and 150 μm, respectively. This implies that the half-length for decay of the bound-state population is approximately 150 μm.

The initial population of levels depends on the angle between the channeling plane and incident-beam direction (the "tilt angle") because the positrons have a larger effective transverse energy at larger tilt angles. As a result, it is reasonable to assume that,

with increasing tilt angle, the levels near the top of a potential well
would be populated preferentially to the levels that are more tightly
bounded.   The LiF crystal provides us with a laboratory in which to
study this effect because, for positrons channeled along the {111}
plane, the n = 2 to 4 levels lie in the "little well" (see Fig. A.1a)
whereas the n = 6 to 9 levels appear in the "big well." The intensities
of the 2→1, 3→0, and 4→3 spectral lines that make up the 45 keV peak in
Fig. A.1b should decrease more rapidly with tilt angle, therefore, t' ∍n
do the 6→5, 7→6, and 9→8 lines that comprise the 30 keV peak. The m̄ ⁻
ured intensity ratio of the 45 and 30 keV peaks as a function of   ⸰
angle is shown in Fig. A.3.   Here, the regions of integration are   ⸗
42.1 to 50.8 and from 23.2 to 38.7 keV, and the entire area under
spectral peaks (including both bremsstrahlung and free-to-bound transi-
tion strength) has been stripped off before integration.   This stripping
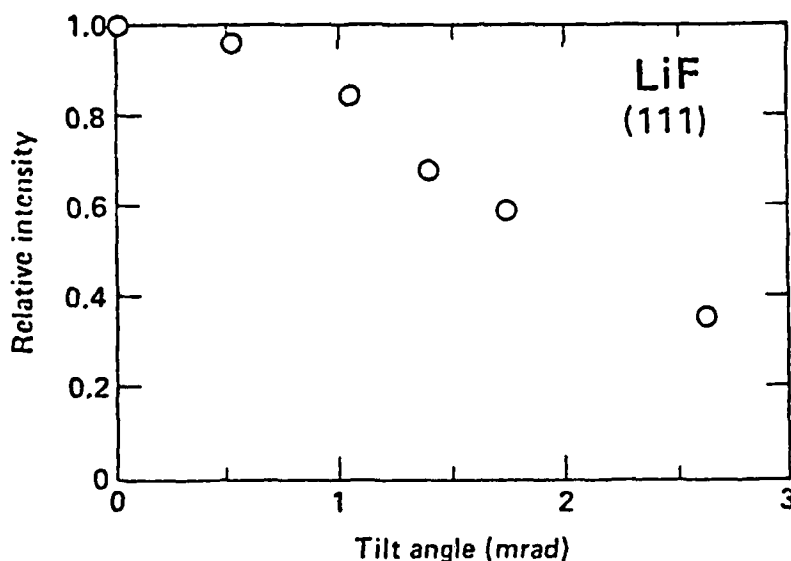
Fig. A.3. MEASURED INTENSITY RATIO OF THE 45 AND
          30 keV PEAKS IN THE RADIATION SPECTRUM FROM 54
          MeV POSITRONS CHANNELED ALONG THE {111} PLANE IN
          LiF AS A FUNCTION OF THE TILT ANGLE BETWEEN THE
          CHANNELING PLANE AND INCIDENT POSITRON BEAM DI-
          RECTION. No error bars are shown because the
          dominant uncertainties are systematic rather
          than statistical.

process introduces a systematic uncertainty (on the order of 10 percent) which substantially exceeds the statistical uncertainty of approximately 10 percent. This ratio drops sharply with tilt angle, as expected.

b.   Positron and Electron Channeling Radiation in Ge

The 54 MeV positrons and electrons were channeled by the {110} planes in Ge, and the data were compared to theoretical predictions for the emission spectrum [10]. Figure A.4a shows a positron channeling-radiation spectrum and the theoretical calculations. This result is in good agreement with theory.

In electrons, however, only a rather broad emission enhancement was observed in the energy range from 30 to 180 keV (Fig. A.4b). Without considering scattering caused by atoms, theory predicts radiation to occur in discrete lines, and this scattering causes the lines to overlap into a single broad line. The scattering probability per unit time varies as the square of the atomic number Z^2 [17] so that, in high Z materials, it is not possible to obtain distinct lines; in contrast, in Si [4], diamond [18], and LiF [12], separate emission peaks were observed because of the lower Z values.
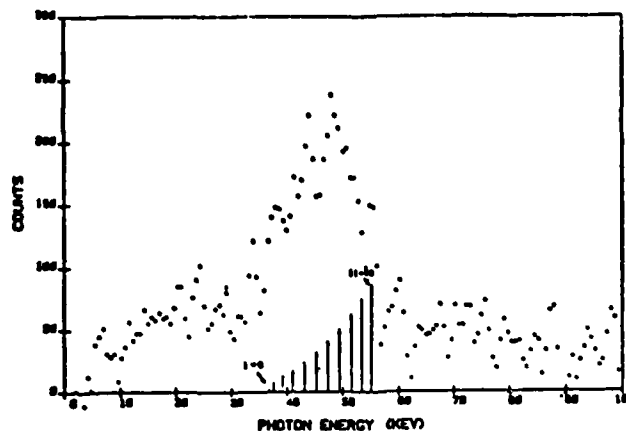
a.   For 54.5 MeV positrons

Fig. A.4.   MEASURED CHANNELING-RADIATION
SPECTRA FOR THE {110} PLANE IN Ge.

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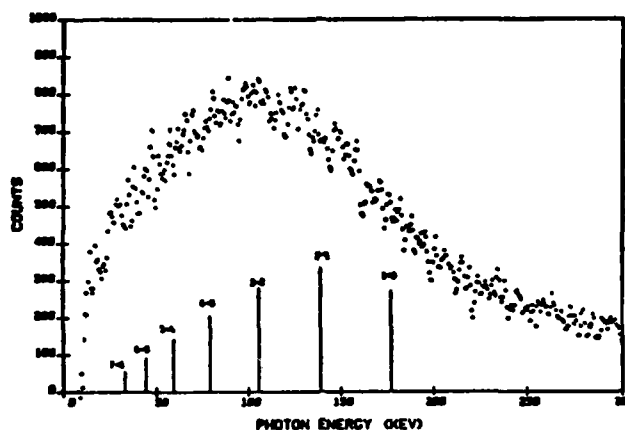
b.   For 54.2 MeV electrons
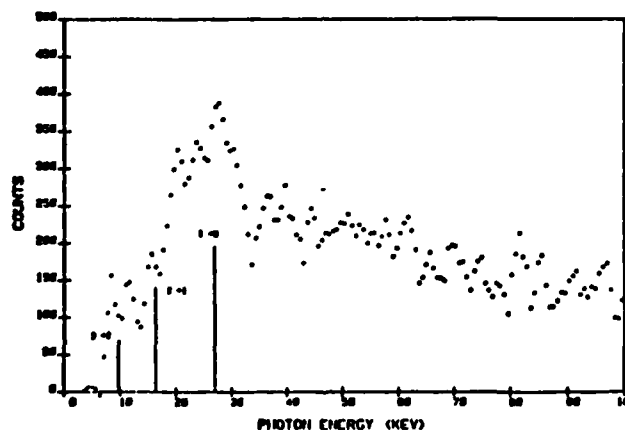
c.   For 16.9 MeV electrons

Fig. A.4.   CONTINUED.

Figure A.4c is the spectrum for electron channeling with 16.9 MeV electrons, and the calculated transitions are included. Because the density of states decreases with lower particle energy, it was hoped that discrete lines could be observed; however, this objective was not realized because, even at 16.9 MeV, broadening caused overlap of the lines.

c. <u>Planar Positron and Electron Channeling Radiation in Diamond</u>

The 54 MeV positrons and electrons were channeled by {100}, {110}, and {111} planes in diamond, and the data were compared to the theoretical calculations [16]. The crystalline potential resulting in channeling radiation can be calculated from any one of a number of models. Figure A.5a plots the potential obtained for positrons channeled by the {111} planes in diamond, using a Hartree-Fock model modified by a Debye-Waller factor to account for atomic thermal vibration. The eigenvalues were derived for 54 MeV particles, based on a many-beam analysis [7] in which Bloch-wave eigenfunctions were substituted into the wave equation. States are numbered, starting with $n = 0$ at the bottom of the well and increasing to $n = 11$ at the top of the well. The highest state corresponding to $n = 11$ is broadened because the energy of the state varies with momentum. Unbound states (above the well and not
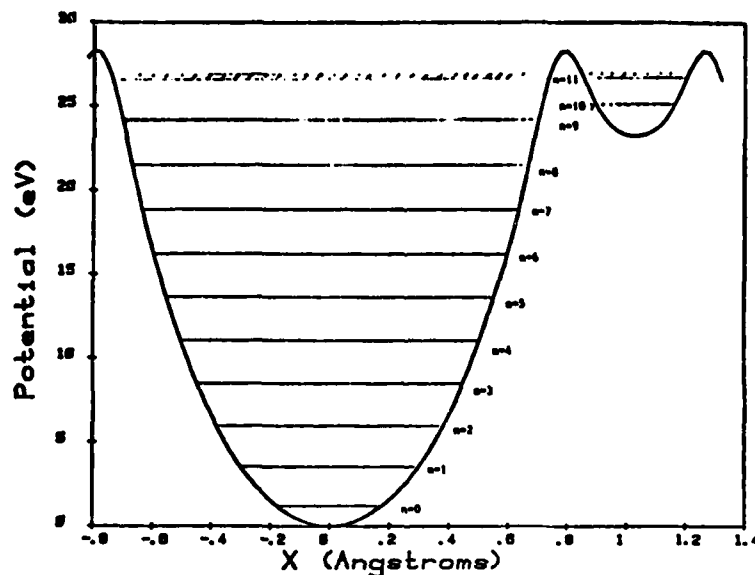
a. Calculated interplanar potentials and eigen-
   states

Fig. A.5. 54.4 MeV POSITRONS CHANNELED ALONG THE
          {111} PLANES IN DIAMOND.
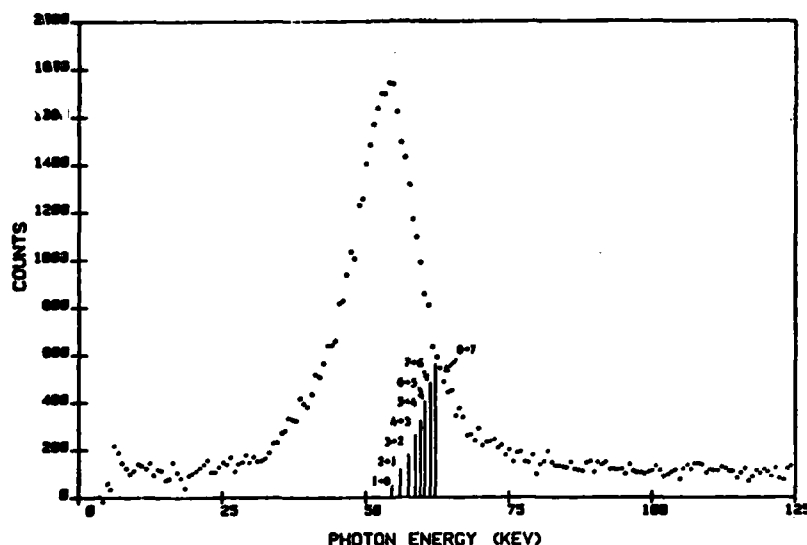
b. Measured radiation spectrum (positrons of the
    vertical lines indicate the doppler-shifted
    transition energies between the eigenstates
    in Fig. A.5a, and their heights indicate the
    intensities of these transitions)

Fig. A.5. CONTINUED.

shown) have progressively broader bandwidths as they approach the free-
particle condition. As can be seen in Fig. A.5a, there are two wells of
different depths because the {111} planes have two interplanar separa-
tions.

        The states near the top of the well have a large spatial
overlap with the atomic planes, which shortens their lifetimes as the
result of nonradiactive transitions induced by atomic thermal vibra-
tions. Not much radiation is expected, therefore, from the states la-
beled n = 9 or higher. Figure A.5b illustrates the channeling-radiation
spectrum with bremsstrahlung subtracted, plus the calculated spectral
lines. Predicted emission lines are approximately 7 percent higher than
the measured line, probably as a consequence of not considering bonding
effects in determining the potential (the potential was obtained by ad-
ding potentials from isolated atoms, and changes resulting from bonding

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were neglected). This error would be fairly significant in diamond because four out of six electrons are involved in the bonding. In Si and Ge where the bonding effects would not be as important, the difference between experimental and theoretical photon energies was only 2 to 3 percent which was within the experimental error.

On the other hand, for electron planar channeling in all three major planes, the experimental results are similar to the predicted emission lines (generally within 3 percent). Because electrons channel close to the atomic planes, in contrast to positrons that channel between planes, the isolated atomic potential is expected to be a more accurate representation for electrons.

Summary of Results

We have measured channeling radiation from LiF crystals, and this is the first time that channeling radiation from a binary crystal was observed. For both {100} and {110} planes, the potentials are close to harmonic and the spectrum has a single peak. The {111} planes, however, have a complicated potential and the channeling-radiation spectrum has four peaks.

The channeling radiation of 54 MeV positrons and electrons was measured in the Ge {110} planes, and the results were compared to the theoretical calculations. The results were found to be in good agreement with theory.

We also measured 54 MeV electron and positron channeling radiation in diamond {100}, {110}, and {111} planes and the results were again compared to theory. The results for electrons were also in good agreement; however, the theoretical model for positrons requires certain modification to account for the bonding effect in diamond.

The platelet effects on channeling radiation are being studied to explain the very interesting line narrowing in the diamond {111} plane.

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     1982.

2.   Submicron Device Physics and Technology

Principal Investigators: J. D. Plummer, C. R. Helms, W. E.
       Spicer/I. Lindau, R. M. Swanson, R. F. W. Pease

This section describes the following five projects that have been chosen as areas for our proposed research:

- Physics and Technology of Submicron Active, Parasitic, and Passive Devices

- Interaction of Arsenic with Silicon Surfaces

- Microscopic Mechanisms in Silicon--Schottky-Barrier Forma-tion

- Ohmic Semiconductor Contacts with Low Minority-Carrier Recombination Velocity

- Failure Mechanisms Associated with Submicron Metallic Interconnections in VLSI

- **Physics and Technology of Submicron Devices** (J. D. Plummer)

Introduction

This research program is divided into three projects which are described separately below, including progress in each area during the past year and an outline of future plans. All three are closely con-nected in that they are aimed at submicron VLSI devices.

In any MOS or bipolar integrated circuit, there are three gener-ic types of structures. The first is the active switching/amplifying device. We are investigating the characteristics of alternative gate

dielectrics for submicron NMOS and CMOS circuits, and thermally grown Si_3N_4 and SiO_2/Si_3N_4 composites appear to have significant advantages over SiO_2. This first project is aimed at evaluating material properties and corresponding device characteristics associated with this alternative dielectric.

The second generic type is a parasitic device and is the result of the local-oxidation techniques commonly used for device-to-device isolation. Such isolation is generally achieved in both bipolar and MOS integrated circuits through selective field oxidation coupled with self-aligned ion-implanted channel stops. Despite its current technological dominance, this isolation technique will be inadequate as device geometries approach 1 μm and, ultimately, submicron sizes. As a result, the scientific objectives of this second project are to (1) use two-dimensional numerical simulation to determine and better understand the limits of local-oxidation device-isolation schemes and (2) investigate, both theoretically and experimentally, isolation techniques that may improve the isolation characteristics at feature sizes of <1 μm.

The third generic type is generally a passive load element which, in bipolar circuits, often takes the form of diffused or ion-implanted resistors. In NMOS circuits, the most common device is a polysilicon resistor. Polysilicon layers are also widely used as gate electrodes and for interconnections in MOS circuits. In this third project, we are investigating the limiting behavior of polycrystalline-silicon layers when they are defined with lateral and vertical dimensions comparable to the grain sizes in the material. Because grain sizes are typically 0.1 to 0.5 μm following high-temperature processes, the dimensions of interest are on the same order as the NMOS channel lengths in the first two projects described above. We plan to analyze in detail the material and electrical properties of a single grain boundary in polysilicon. All current models of polysilicon properties rely on the statistically averaged behavior of many grain boundaries in series; however, in small-geometry structures, this will not be a reasonable assumption.

In summary, we are engaged in a coherent investigation of the problems of submicron silicon integrated circuits, and the three projects are aimed at the three key components of any modern silicon circuit. Our intent is to establish a scientific basis for understanding and circumventing problems that may occur in scaling the three generic structures to submicron dimensions.

a.   **Alternative Gate Dielectrics for Submicron MOS VLSI**
       (M. Moslehi, K. C. Saraswat, J. D. Plummer)

Scientific Objectives

Very thin gate insulators are required for scaled devices in advanced VLSI device structures. Thinner gate insulators in combination with optimized device design eliminate many undesirable second-order effects, such as short and narrow channels, drain-induced barrier lowering, and hot carrier trapping; application of very thin gate insulators to IGFETs also improves their radiation resistance and reduces the threshold voltage shift of scaled devices resulting from heavy substrate-doping concentrations. The application of these gate insulators also increases the density of mobile carriers in the channel for a given gate voltage, which reduces alpha-particle disturbances in scaled structures.

Thermally grown silicon-nitride and nitride-oxide (nitroxide) films are becoming promising candidates for the fabrication of very thin gates in VLSI devices [1] and are superior to thermal SiO_2 films in VLSI devices and technology [1,2] for many reasons. They have higher density and permittivity than do SiO_2 films, excellent masking against oxidation and impurity diffusion, and better breakdown uniformity can be expected because of improved resistance to alkali ion migration. Thin-gate SiO_2 films ($\simeq$200 Å) can deteriorate during VLSI processes, such as refractory metal or silicide gate deposition or annealing, or during ion or plasma-assisted processes; however, thin nitride and nitroxide films are not damaged by them. In addition, improved characteristics have been reported for nitride gate devices [2]. Processes such as forming-gas

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annealing reduce the breakdown field of very thin SiO_2 films but not those of nitride and nitroxide films. As a result, it is believed that these thermally grown films will be important materials for future submicron VLSI devices.

The major kinetic difference between thermal nitridation and thermal oxidation is based on the higher structural density of the thermal nitride. This results in a self-limiting growth property for the thermal-nitridation process using ammonia. Figure A.6 plots the typical dependence of thermal-nitride thickness on nitridation time in ammonia and temperature and the variation of the final saturated thickness with temperature [3].
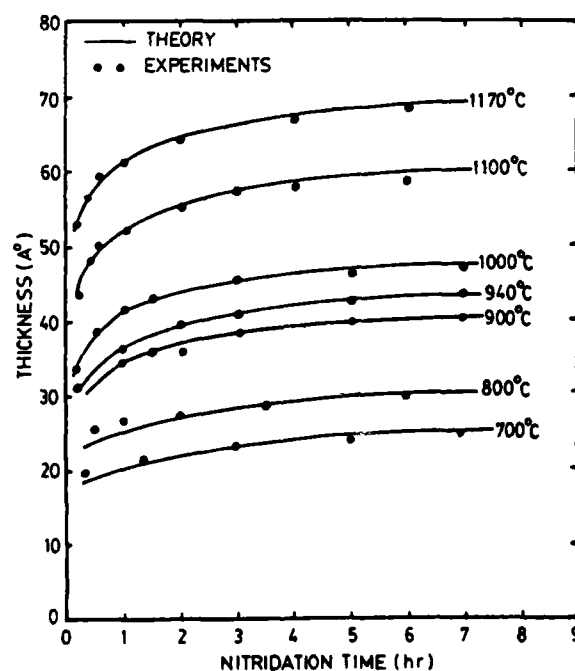
Fig. A.6. COMPARISONS OF THE GROWTH-
RATE DATA OF AS-GROWN THERMAL-NITRIDE
FILMS AND THE THEORETICAL MODEL [3].

This self-limiting growth property is an important advantage of thermal nitrides in semiconductor devices in which thin insulator films with high purity and precise thickness control are required.

The saturated thickness of the thermal nitride is expected to be a
function only of nitridation temperature and not the partial pressure
and flow rate of ammonia [3,4].

Progress

This research began with the setting up of special-pur-
pose experimental equipment for thermal nitridation. Uniform silicon-
nitride and nitroxide films (~50 Å) are being thermally grown with pure
ammonia in a modified expitaxial reactor.

The composition, thickness, refractive index, interface,
and electrical characteristics of these films are being studied through
ellipsometry, RBS, AES, SEM, and C-V techniques. Their uniformity has
been analyzed under various growth conditions as described below.

The experimental apparatus is a Hier II epitaxial reactor
modified to produce flow rates ranging from 1 to 10 lit/min of 100%
ammonia as shown in Fig. A.7. All nonmetallic seals in the ammonia gas
flow must be made from special materials to prevent degradation in high-
concentration ammonia. Most CVD reactors do not meet this condition
and, therefore, are not suitable for this work. Our thermal nitridation
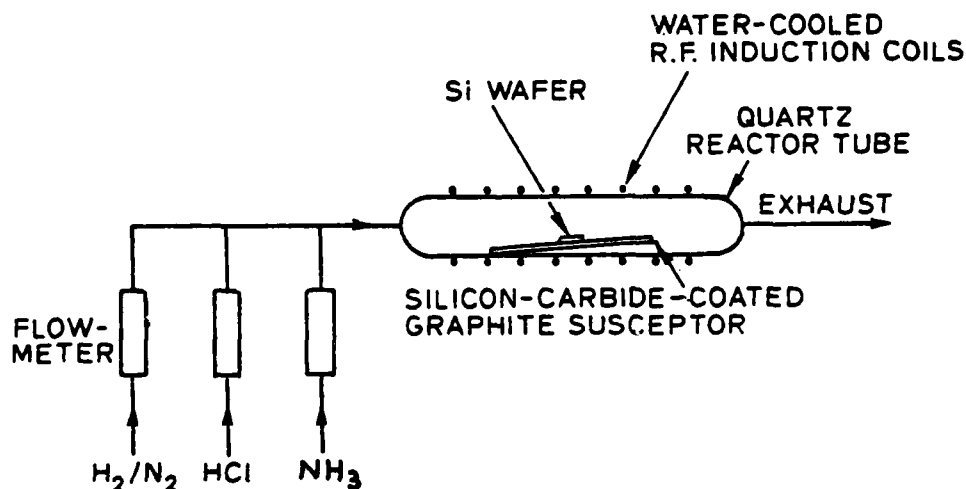
Fig. A.7. EXPERIMENTAL APPARATUS FOR THE GROWTH OF THERMAL-
           NITRIDE LAYERS.

made use of a cold-wall process because of RF heating and, as a result, oxygen contamination of the nitride films caused by the nitridation tube has been avoided.   A modified epitaxial reactor enabled in-situ HCl etching prior to growth to improve the quality of the thermally grown films.

A series of six experiments has been completed to evaluate the experimental apparatus and to refine the film-growth techniques. The first run (t = 4 hr, T = 1100°C, flow rate = 1.8 lit/min) produced films with extensive surface pitting.   The improved appearance of the surfaces resulting from the next two runs tends to support the conclusion that the severe pitting in the first run was partly the result of a transient condition--most likely the presence of contaminants in the experimental reactor.   In the first runs, microdefects (such as pitting) resulted in high surface-field concentrations, leakage, and breakdown-field reduction and, consequently, the C-V data obtained from the first series of experiments were of limited value.   Capacitor depletion, accumulation, and breakdown voltages were identifiable on the plots.   Because of the use of high-resistivity substrates ($\approx$16 Ω-cm) and leakage produced by microdefects, the inversion and deep depletion capacitances were almost equal and no quasi-static measurement was possible.   Because all films resulting from the first experiments showed pitting to depths greater than 1 μm (SEM results), the ellipsometer data were erratic, and no C-V measurements were obtained in the first run;   wafers with <111> orientation showed significantly more pitting.

Before our recent improvements in nitridation growth conditions, the breakdown voltage for 55 Å thermal-nitride films was approximately 3 V which corresponds to a breakdown field of 5.5 MV/cm. We believe that the breakdown characteristics can be improved by a factor of 2 by improving the nitridation-process conditions.

In subsequent experiments in 100% ammonia at 1100°C, 45 to 60 Å of thermal-nitride and nitroxide films were grown at nitridation times between 1 and 4 hr and for various substrate resistivities and orientations.   These runs were directed toward isolating and eliminating the pitting problem and improving the electrical characteristics of the

films. We have been successful in eliminating the pitting problem, and very uniform thin thermal silicon-nitride films have been grown with very little pitting. This has been achieved by improving the nitridation apparatus and growth conditions and by using ammonia gas with reduced O_2 and H_2O contamination ($O_2 < 1$ ppm, $H_2O < 1$ ppm).

It is well known that chemical cleaning procedures (including standard prefurnace cleaning) leave trace contaminants on the wafer surface. In our last experiments, we improved the quality and stoichiometry of the thin thermally grown nitride films by removing these contaminants by in-situ etching with HCl before nitridation. Stoichiometry was improved by removing the native oxide layer prior to nitridation. A film-thickness nonuniformity of less than 5 percent was obtained for each wafer.

Summary of Results

Initial experiments in thermally growing Si_3N_4 films have been successful. These films are being characterized for possible application as thin gate dielectrics in NMOS and CMOS VLSI structures. Future work will include investigation of the mechanical properties of the films and detailed studies aimed at a better understanding of growth kinetics.

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b.   Isolation Techniques Suitable for Submicron Technologies
     (S. H. Goodwin, J. D. Plummer)

Scientific Objectives

        In N-channel MOS technology, device isolation is commonly
achieved by ion implantation of the field region followed by local oxi-
dation to form a thick field oxide. The active-device regions are pro-
tected from these steps by a masking layer of silicon nitride which is
subsequently removed. This technique, illustrated in Fig. A.8, has the
following advantages.

- The field oxide is self-aligned to the more heavily doped
  channel-stop region.

- Ion implantation protects against field surface inversion
  and provides an optimal choice of substrate doping for the
  active devices.

- Overall packing density increases by applying the field
  oxide as a portion of the drain/source mask.

- Because local oxidation consumes silicon, the step-height
  difference between the field and device regions is reduced.
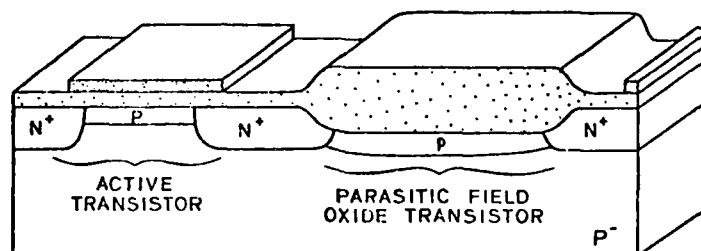
Fig. A.8. CROSS SECTION OF A CHIP CONTAINING
    AN ACTIVE TRANSISTOR AND A PARASITIC FIELD-
    OXIDE TRANSISTOR. The parasitic transistor
    is between the active transistor on the left
    and another on the far right. The relatively
    thick-oxide and high-substrate (P-implant)
    doping levels produce relatively poor sub-
    threshold slopes in the parasitic device so
    that device-to-device isolation is best char-
    acterized by the leakage (subthreshold) cur-
    rent that flows for a given gate voltage.

The principal disadvantage is the chip area consumed. Because of the lateral diffusion of the channel stop and lateral oxidation (bird's beaking), the electrical length of the channel-stop region is significantly larger than the mask dimension.

The objective of this project is to investigate device-isolation techniques that would best resolve this problem. There are two thrusts in this investigation. One is to examine the limits of current technology as it is scaled down; the other is to analyze alternative isolation techniques to determine their limits in comparison to today's technology, including approaches recently suggested in the literature [1,2,3].

Progress

Extensive work on these problems has been done with a two-dimensional device-simulation computer program, GEMINI [4]. The first series of simulations compared two variations of the local-oxidation technique; one was the partially recessed structure in Fig. A.9a (no silicon etching), and the other was the fully recessed structure in Fig. A.9b (silicon etched in the field regions to yield a planar oxide surface). Comparison of the I_D vs V_{GS} curves of these two devices revealed that the second had better isolation properties.

To obtain a deeper understanding of the operation of the fully recessed structure, we simplified it and simulated a thin uniform-oxide device with the same oxide/semiconductor interface geometry. These simulations indicated that the corner of the oxide near the source has beneficial two-dimensional effects. The gate voltage must support charge in a pie-shaped region of the semiconductor larger than an analogous planar region. Less band bending is required, therefore, to uncover the necessary bound depletion charge that generates a peak in the potential along the channel. There are effectively, then, three devices in series—two corner devices and a planar device between them (see Fig. A.10).
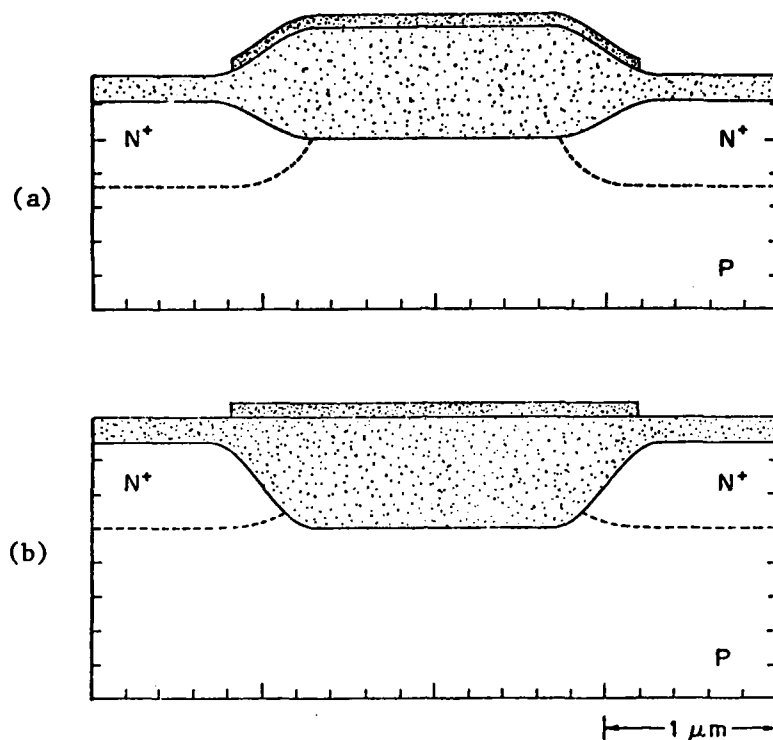
Fig. A.9. SEMI- AND FULLY RECESSED ISOLATION-REGION
           STRUCTURES.

        The potential barrier that now controls the current is
located at the corner of the oxide near the source and has moved from
its normal position at the planar region of the structure. This implies
that the channel can be shortened without degrading the isolation prop-
erties of the device. For the corner effect to occur, it must be part
of the region controlled by the gate and, as a result, the metallurgical
boundary of the source and the depletion region controlled by the source
must be above the corner.

        Having gained an understanding of the basic mechanism of
the corner effect, we returned to an isolation-type structure to deter-
mine how this effect can be applied. As has been noted, the depth of
the source/drain junctions is critical. As they are pulled up toward
the surface, the corners are more exposed and become part of the gate-
controlled channel, which leads to larger potential barriers at the
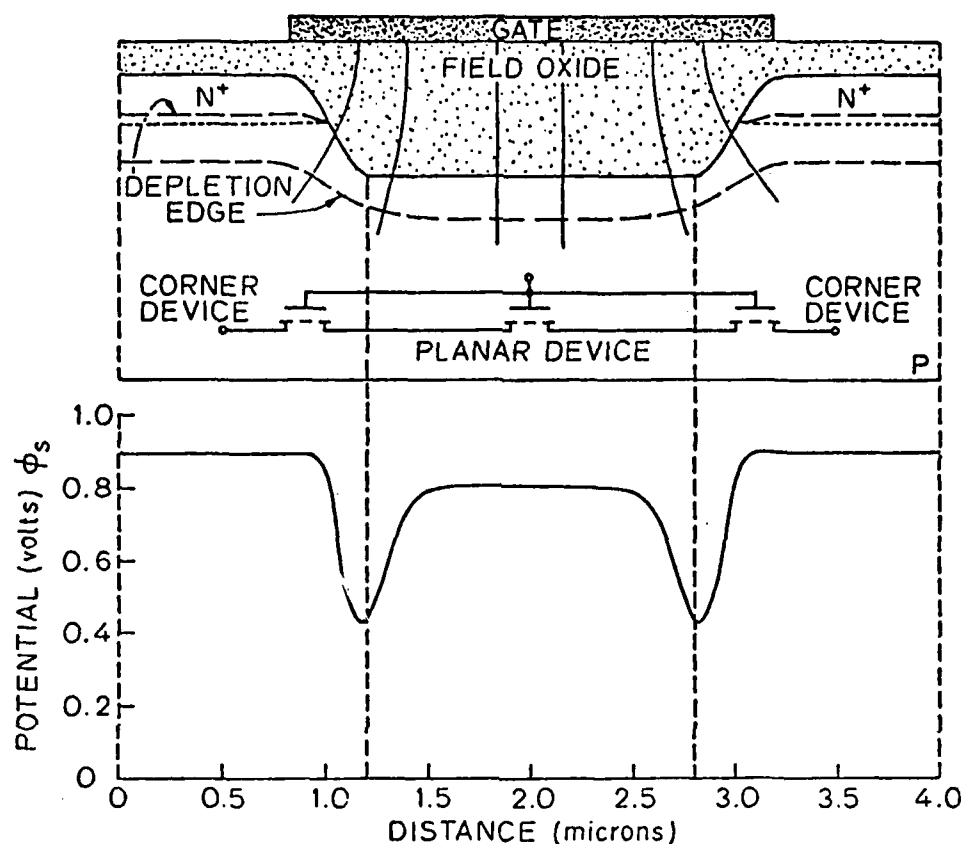
Fig. A.10. THE SOURCE/DRAIN JUNCTIONS PULLED UP TO EXPOSE THE
CORNERS OF THE OXIDE. The gate is biased for 1 pA/μm. The
potential barriers are now at the corners of the oxide. V_S,
V_D, V_{SUB} = 0, V_G = 18.5, N_A = 2 $\times$ 10^{16} cm^{-3}. Simple one-di-
mensional MOS theory predicts the potential barrier height in
the center region (planar device). Two-dimensional effects
caused by charge sharing in the corner regions produce a sub-
stantially larger potential barrier height, and this barrier
height actually controls leakage current in the device; it
can be optimized through geometry and junction depth.

corners. The I_D vs V_{GS} curves shift to larger voltages and the slopes
are reduced, and this results in better isolation. The curvature of the
corner also plays a major role. A smaller radius at the interface pro-
duces a larger peak in the potential and thus improves isolation. The
addition of a back-gate bias also enhances the corner effect. The addi-
tional gate voltage required for the extra band bending changes the

surface potential less at the corner than in the planar region, thereby heightening the corner effect. Because changes in doping affect this technique in different ways, the overall effect will depend on the particular structure. Heavier doping pulls up the depletion edges of the source and drain and results in a greater corner effect; it also results in a thinner depletion region around the corner, which reduces the two-dimensional aspect of the corner and lessens its effect. Heavier doping requires a higher gate voltage, and this larger voltage increases the corner effect because of the geometry of the oxide.

Simulations to investigate shorter channels verified that the corner effect reduces the well-known short-channel degradation of device characteristics. Devices with sharp corners (right angles) had the best characteristics at the shortest channel lengths. With short enough channels, control of the potential barrier shifts from the gate to the drain. This results in perfectly flat I_D vs V_{GS} curves, with the drain current determined by V_D and the distance between the corner and the drain.

We have designed and constructed a set of masks that will enable us to verify the corner effect experimentally. Devices of varying channel lengths and widths have been fabricated, including the Canon FPA 141 projection-alignment system purchased under JSEP support FY 78. The devices were realized on <110>-oriented silicon wafers with a KOH etch to produce vertical sidewall grooves that were later oxidized to form the field oxide. Initial experimental measurements (Fig. A.11) verified the basic advantages of the corner effects, and further experiments are under way to optimize the isolation region.

Summary of Results

By computer simulations, an important two-dimensional corner effect has been identified and investigated. This effect is a controlling potential barrier near the source of a device at the corner of the oxide, which is the result of the reduced linkage between the gate voltage and surface potential. This barrier achieves dramatic

EXPERIMENTAL RESULTS
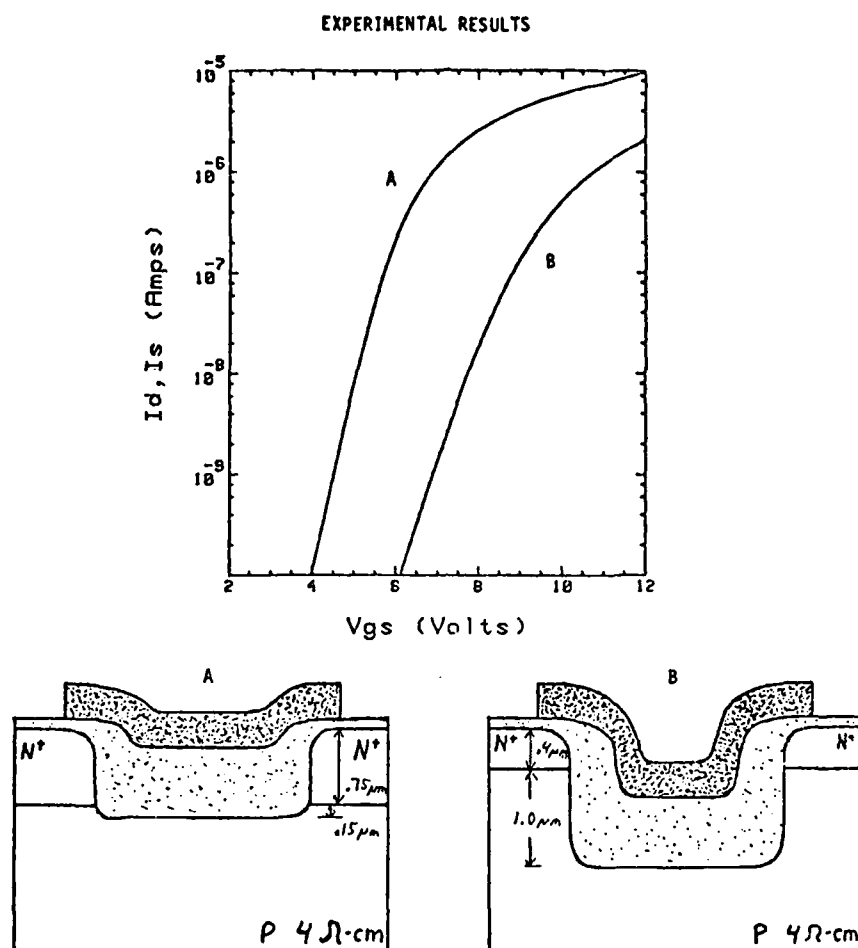
Fig. A.11. A TYPICAL EXAMPLE COMPARING DEVICES WITH (B)
AND WITHOUT (A) THE CORNER EFFECT. This effect reduces
the current by a factor of 10^3 at a given gate voltage.
A lateral shift of the curves and a change in slope can
be seen. The substrate is uniformly doped at 3.5×10^{15}
cm^{-3} to illustrate the improved isolation without any
field implant. $V_{DS} = 0.05$ V, $V_{SUB} = 0$ V, $W = 500$ μm,
$L = 40$ μm, $t_{ox} = 7000$ Å.

improvements in isolation. Devices have been fabricated to verify this
effect experimentally.

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    c.   Electronic Properties of Polysilicon Grain Boundaries
        (D. B. Kao, K. Saraswat, L. Gerzberg)

Scientific Objective

The objective of this study is to investigate the electronic structures of grain boundaries in polysilicon by controlling the amount of incorporated atomic hydrogen through hydrogen implantation. Our research has been divided into three areas--problem definition and literature survey, design of experiments, and the design of test-chip masks.

Progress

Polycrystalline silicon is a versatile material in IC processing. It has a wide range of resistivity that can be varied by impurity doping and electric field. It can tolerate high-temperature processing and is compatible with silicon technology. Because of these advantages, polysilicon has been used as a resistor, conductor, insulator, dopant source, and a fuse for PROMs.

The electrical properties of polysilicon are dominated by the grain boundaries that serve as the interface between two crystalline grains with different orientations [1,2,3]: The lattice irregularities and dangling silicon bonds generate the localized energy states that can trap mobile carriers and become charged. These charged localized states result in a potential barrier that impedes the conduction of mobile carriers. Understanding the electronic structures of the localized states

in the grain boundaries is the key, therefore, to controlling the conductivity in polysilicon.

Atomic hydrogen has been known to passivate the dangling bonds and reduce the localized states. Hydrogen anneal of MOS transistors is a standard processing step. Implantation of hydrogen makes possible the fabrication of MOS transistors with extremely low interface state density [6]. Hydrogenation is necessary in the fabrication of devices in amorphous silicon because it reduces the localized states and facilitates effective dopant incorporation.

The resistivity and optical properties of polysilicon are also affected by hydrogen [4,5]. In our initial experiments, it was observed that the presence of hydrogen reduces the resistivity in lightly doped n-type polysilicon and increases it in lightly doped p-type polysilicon. The data indicated that the change in resistivity increases as the amount of hydrogen is raised.

To investigate the detailed electronic structures of grain-boundary localized states, the amount of hydrogen must be controlled. We plan to implant hydrogen into devices fabricated in polysilicon and to measure their electrical properties. By measuring the density of localized states in polysilicon capacitors implanted with different amounts of hydrogen, we hope to determine the energy distribution of these states. By varying the amount of hydrogen and dopant concentration in polysilicon resistors, we can determine the effects of the localized states on the conductivity of polysilicon. This understanding could lead to the fabrication of well-controlled polysilicon resistors.

Based on the above considerations, we have developed experiments to fabricate capacitors and resistors in polysilicon. These devices will include

- capacitors of different sizes and area-to-peripheral ratios

- capacitors with metal-oxide-polysilicon and metal-oxide substrate structures

- capacitors with metal-oxide-polysilicon and metal-polysilicon-oxide substrate structures

- resistors of different sizes and width-to-length ratios

- resistors with control gates

- Van der Pauw structures for resistivity measurements

The two major variables in the processing schedule are the amount of implanted hydrogen in the polysilicon and dopant density.

To achieve better control of the quantity of hydrogen, we will use silicon nitride and oxide in some of the runs. To avoid hydrogen generation through aluminum/water reaction, we will apply a titanium-tungsten alloy instead of aluminum for the plates and contacts. Our test chip will also include diodes of different sizes and junction lengths and MOSFETs with various sizes, channel widths, and width-to-length ratios.

Summary

We have completed the design of the masks (on an Applicon 860 graphics system) for the test chip, and a set of masks has been made for the Canon FPA-141F 4:1 reduction fine-pattern projection mask aligner. We have begun preliminary work on fabricating the test chip.

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● **Interaction of Arsenic with Silicon Surfaces** (C. R. Helms)

   Scientific Objective

   Dopants at semiconductor interfaces are of vital interest to the
silicon device-processing industry. High concentrations of dopants are
known to be present at semiconductor interfaces caused by interfacial
segregation of these impurities from the bulk, and the interaction
between the segregated dopants and interface may impact the electrical
properties of both the interface and dopant. These dopants may strongly
influence the position of the Fermi level within the band gap and the
corresponding electrical-barrier heights.

   In the studies reported here, monolayer quantities of arsenic
and boron are deposited on the silicon surface under ultra-high vacuum
conditions and changes in the electronic structure are observed.
Although the free silicon surface is not a practical device interface,
the distinct advantage of this interface is the ready application of
surface-sensitive electron spectroscopies. The experimental results are
compared to a theoretical Xa-SCF calculation of the electronic structure
of arsenic surrounded by a tetrahedrally coordinated sphere of four
silicon atoms.

   Progress

   The principal experimental technique employed in this study is
ultraviolet photoemission spectroscopy (UPS). The surface electronic
structure and the surface position of the Fermi energy within the gap
are determined by UPS in terms of the optical density of states of the
valence band. Photoemission spectra at a photon energy of 10.2 eV were
used for this study because the electronic structure near the valence-
band maximum is more pronounced at this energy. Spectra were obtained

30

from the surface of clean sputter-annealed Si (100) and after deposition and annealing of either arsenic or boron.

Arsenic can be deposited from arsine gas onto an atomically clean lightly doped p-type Si (100) surface [1]. Penetration of arsenic into the subsurface region can be achieved by relatively long high-temperature anneals in an arsine ambient. The arsenic-surface coverage saturates at ≈10% of a monolayer, and relatively small amounts of arsenic are incorporated beneath the surface. The strong influence of the subsurface arsenic is apparent in Fig. A.12 as a downward shift in the silicon valence band by roughly 0.3 eV without a significant change in the sample work function [2]. The absence of surface states and the large increase in emission at -2 eV can also be seen. Arsenic deposited on the surface with a minimum high-temperature anneal does not result in a shift of the bulk silicon peaks.

The effect of boron on the silicon-surface electronic structure was also investigated with UPS. Boron was deposited on lightly doped n-type silicon at room temperature by E-beam evaporation, and the sample was annealed at high temperatures to incorporate the boron into the subsurface region. The effect of the subsurface boron (Fig. A.13) is an upward shift in the silicon valence band. This subsurface boron does not significantly change the work function as indicated by the unchanged energy cutoff near -5 eV.

The addition of donors and acceptors to the silicon surface was observed to shift the valence band toward lower and higher binding energies, consistent with dopant behavior in the bulk. The absence of correlating work-function deviations with shifts in the bulk Si peaks indicates that the subsurface dopants strongly change the band bending without significantly varying the Fermi pinning position. The initial and final conditions of band bending, consistent with the experimental data for a lightly doped p-type substrate, are shown in Fig. A.14 by the long thermal anneals in an arsine ambient. The band bending induced by boron on an n-type substrate is similar except the direction of band bending is reversed.
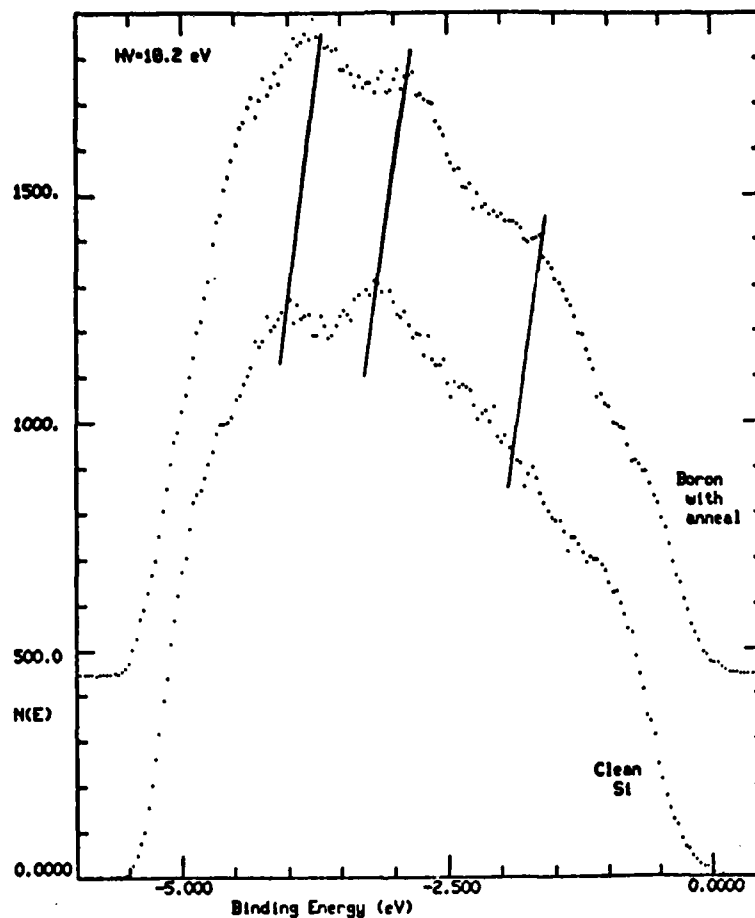
Fig. A.12. PHOTOEMISSION SPECTRA OF THE CLEAN p-
TYPE SURFACE AND AFTER A HIGH-TEMPERATURE ANNEAL
IN 1.5×10^{-7} TORR ARSINE. The slanted vertical
lines emphasize the energy shift of the peaks.

A theoretical approach to achieving an understanding of the
electronic structure of these local nonperiodic geometries is the linear
combination of atomic orbitals (LCAO). An effective computational
implementation of this LCAO method for polyatomic clusters is provided
by the self-consistent field/scattered-wave technique with the Xa sta-
tistical approximation to exchange the correlation (Xa-SCR) [2]. The
clusters used in these spin-restricted nonrelativistic calculations are
constructed with nonoverlapping spheres with a radius equal to one-half
the nearest-neighbor distance in bulk silicon. The cluster-wave

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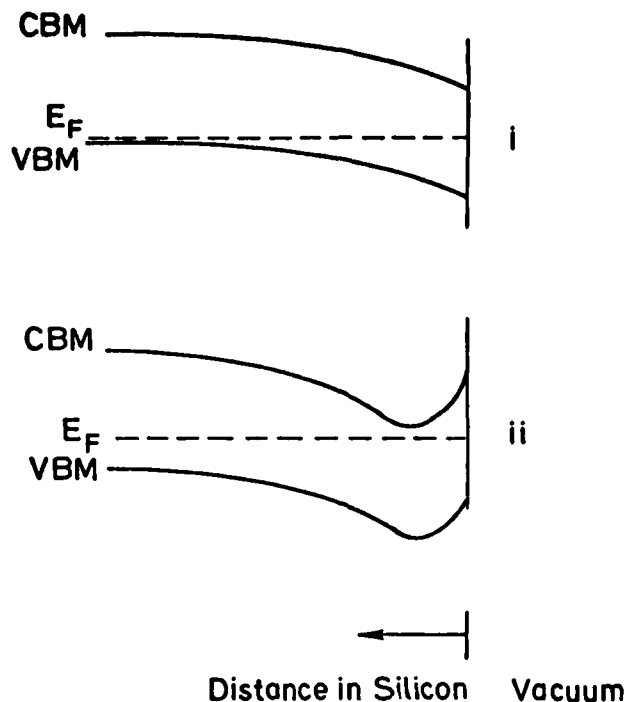
Fig. A.13. PHOTOEMISSION SPECTRA OF THE
CLEAN n-TYPE SURFACE AFTER DEPOSITION
OF A FEW MONOLAYERS OF BORON AND A
HIGH-TEMPERATURE (1200°C) ANNEAL FOR
1 MIN. The slanted vertical lines em-
phasize the energy shift of the peaks.

functions are expanded into a large set of spherical harmonics. All representations of the point group T_d contain an s, p, or d component or any atom.

The discrete energy levels for the molecular orbitals of the Si_5 and Si_4As clusters are identified by their symmetry and are broadened with a gaussian to yield the density-of-states plot in Fig. A.15. The 20 valence electrons of the silicon cluster fully occupy the lowest-lying molecular orbitals in the order of increasing binding energy $1A_1$, $1T_2$, $2A_1$, $2T_2$, and E. The additional electron in the Si_4As cluster resulting from the central arsenic atom is placed in the next available $3T_2$ level. The arsenic-induced shift of the molecular orbitals to greater binding energy is readily understood in terms of the more

33
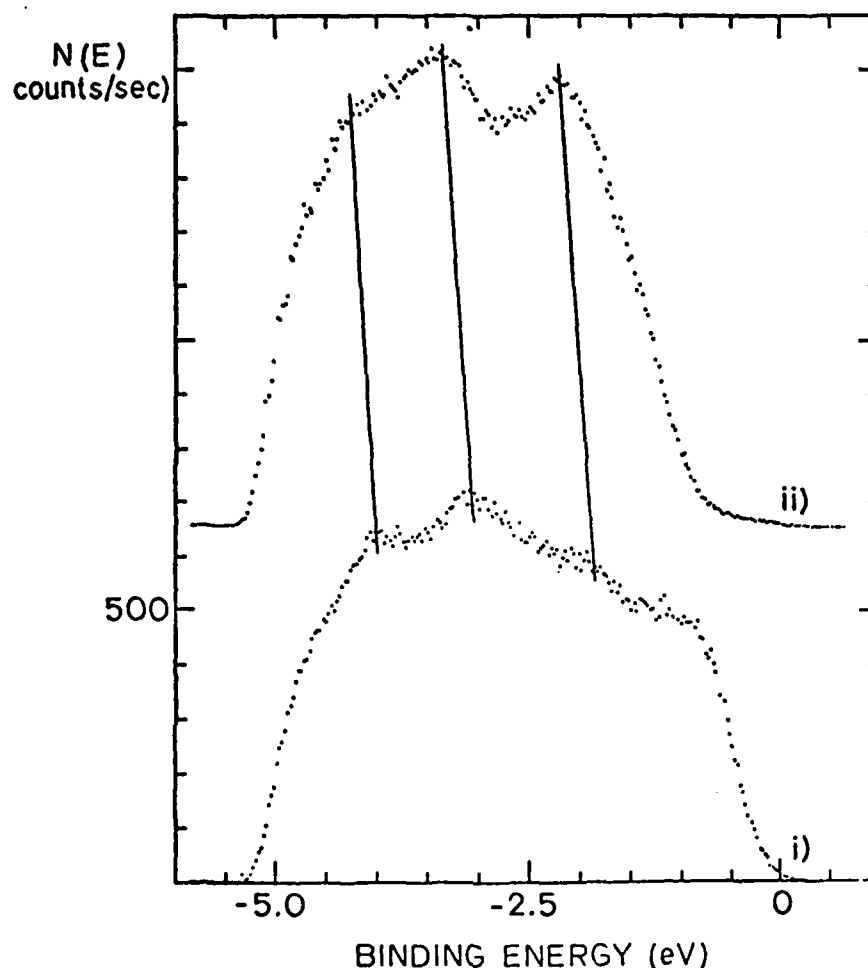
Fig. A.14. BAND DIAGRAM SHOWING FERMI-ENERGY PINNING AND
    BENDING OF THE VALENCE-BAND MAXIMUM AND CONDUCTION-BAND
    MINIMUM WITH DISTANCE INTO THE BULK NEAR (i) THE CLEAN
    SILICON SURFACE AND (ii) THE SURFACE AFTER INCORPORA-
    TION OF ARSENIC BY ANNEALING IN AN ARSINE AMBIENT.

attractive arsenic-core potential. The Herman-Skillman atomic binding
energies for the arsenic 4s and 4p electrons are -14.9 and -5.9 eV and,
for the silicon 3s and 3p, they are -11.7 and -5.3 eV, respectively.
Consequently, the two electrons in the $1A_1$ level undergo the largest
shift because they are composed of s electrons on the central atom. The
six electrons occupying each filled T_2 level are comprised of p elec-
trons, and the four electrons in the E level are a combination of s and

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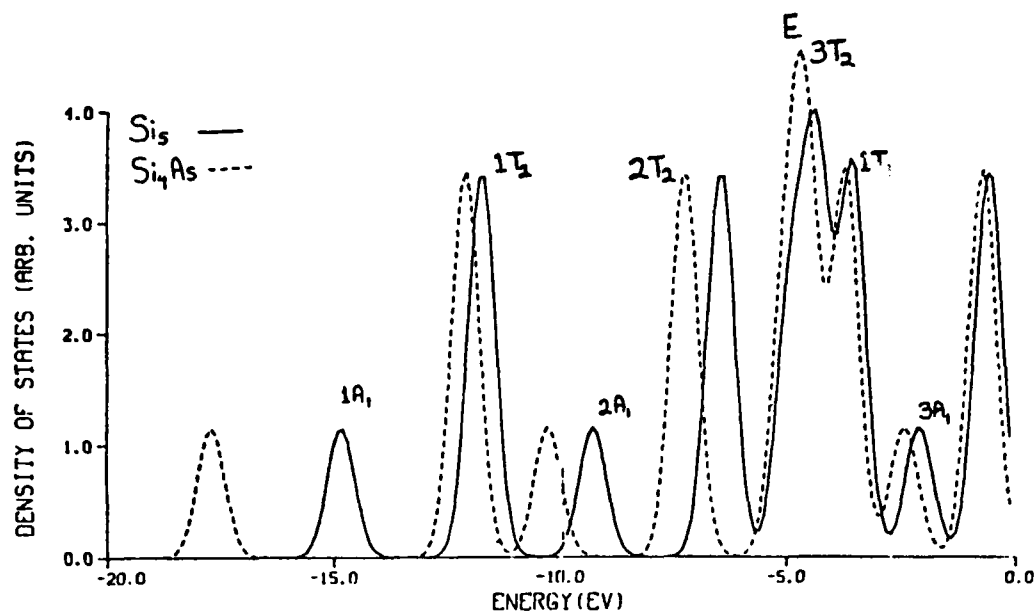
Fig. A.15. DENSITIES OF STATES FOR THE Si_5 AND Si_4As CLUSTERS.
The labels adjacent to each orbital correspond to an irreducible
representation of the T_d point group.

p electrons. The highest concentration of arsenic p electrons is lo-
cated in the $2T_2$ level. The photoemission cross section for the arsenic
4p electrons is approximately 20 times greater than the silicon 3p cross
section at a photon energy of 21.2 eV. As a result, arsenic-derived
features in UPS spectra should appear at the binding energy of the $2T_2$
level. Indeed, a region of increased emission intensity was experimen-
tally observed 2 eV below the Fermi energy by depositing arsenic from
arsine gas onto a silicon surface. The agreement between experiment and
these calculations is favorable.

The size of the Si_5 and Si_4As clusters used in these calcula-
tions is small, and the arsenic-induced level is not associated with the
dangling surface bonds. One method for distinguishing between the bulk
molecular orbitals and the surface-related orbitals is to plot the cen-
tral atomic component of each molecular orbital. This procedure yields
the local density of states (LDOS) at the central atom. The E and $3T_2$
levels are nearly completely absent because these orbitals are located

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on the outer ring of the cluster. The $2T_2$ levels is the orbital with the greatest content of arsenic p electrons and is not attenuated by the LDOS procedure; consequently, the arsenic-derived level is characteristic of bonding in the silicon bulk.

Summary of Results

The results of this investigation are as follows.

* Donors interact strongly with Si surface states, leading to states outside the band gap.

* The surface Fermi-level position remains relatively unchanged with dopant adsorption, and the major effect is the result of subsurface dopant incorporation.

* Donor interaction was verified by theoretical calculations of the electronic structure of Si-As clusters.

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* Microscopic Mechanisms in Silicon--Schottky-Barrier Formation (W. E. Spicer, I. Lindau)

Scientific Objectives

During the last year, this program has been directed toward the development of

* systematic and microscopic understanding of the interactions between silicon, impurities, and metals

* quantitative criteria for the variations in Schottky-barrier performance vs specific amounts of common contaminants

- models of the effect of contaminants on Schottky-barrier performance

Progress

We have extended our investigation of the electronic structure of the cleaved semiconductors (Si, Ge) to the d-metal interfaces to cover all the noble and near-noble Si junctions and to the d models with lower d-shell occupancy (Mo/Si). The Cooper-minimum method for photo-emission with synchrotron radiation for 4d and 5d metal/semiconductor interfaces and a combination of photoelectron and Auger-lineshape spectroscopies for the 3d interface (Cu/Si) enabled us to obtain precise assignments of the orbital characters of the various constituents to the total density of states at such interfaces and, therefore, to decide chemical bonding.

Summary of Results

We introduced the use of known (calculated) subshell cross sections for photoionization to estimate the composition of the interface products. For example, we can detect the formation of Cu_3Si at the Cu/Si interface at room temperature. Our work has broadened the knowledge of semiconductor metal systems and contributed to a deeper understanding of the nature of their chemical bonding and kinetics at the interfaces. More than ten scientific papers on this topic have been completed during the year.

- ### Ohmic Semiconductor Contacts with Low Minority-Carrier Recombination Velocity (R. M. Swanson)

Scientific Objective

Our research has been directed toward the development of metal-silicon contacts with low minority-carrier recombination velocity.

Progress and Results

The thin diffused layers in microelectronic circuits are generally transparent to minority carriers. As a result, the properties of many devices, particularly bipolar transistors, are partially controlled by recombination at the metal/semiconductor interface. Projections of device geometries indicate that such recombination will assume greater importance in the future. An emitter junction cannot be made too shallow, or contact recombination will reduce its efficiency; making it deep, however, minimizes basewidth controllability and reduces speed because of emitter charge storage.

Reducing the minority-carrier recombination velocity at the metal/semiconductor interface would enhance device performance. Such an effect has been observed where current gain was greatly enhanced in transistors utilizing polysilicon contacts to the emitters. Whether this is the result of an interfacial oxide-like layer that presents a tunneling barrier to minority carriers or whether it is caused by a lower diffusion velocity or some other bulk-related property has not been resolved.

The addition of oxygen and dopant to the polysilicon films during deposition produces a silicon oxide of nonstoichiometric composition. With a suitable annealing procedure, these SIPOS films (semi-insulating polycrystalline silicon) have displayed beta enhancements greater than those observed for polysilicon contacts to the same device structure.

Devices fabricated using the first mask set displayed a significant reduction in the emitter saturation current. The beta enhancement for SIPOS and poly contacts was 4.7 and 1.7, respectively, when compared to the metal-contact devices; however, because no optimization was attempted with regard to the processing parameters of either film, their relative merits are not certain.

To facilitate the direct measurement of the effective surface recombination velocity as seen by minority carriers in Si at the contact interface, a second-generation mask set was designed. This mask set

extends the capabilities to extract the emitter saturation current by refining the parasitic base-current extraction procedure. Provision for three simultaneous emitter diffusions enables verification of device modeling for the various profiles. Devices with varying contact-window areas and guard rings indicated that the bulk of the base-defect component stems from recombination at the surface of the emitter periphery. By incorporating these structures in future devices, it should prove possible to extend the range where the reverse-injection component dominates base-current behavior.

The most recently completed device run attempted to ascertain if interfacial or bulk properties were the dominant mechanism for beta enhancement when different contact schemes were used. Polysilicon emitters of varying thicknesses, but processed identically, were used to determine whether the physics of minority-carrier transport in these conceptually simpler films could be verified and to serve as a guide to the understanding of the corresponding mechanisms in the SIPOS films. The presence of trace contaminants in the poly (most likely, O_2), as indicated by the etching properties of these films, made these results inconclusive. The poly-deposition process is being examined to establish whether this is a problem inherent to the current scheme (low temperature, in-situ doping) or whether the system is the victim of extrinsic contamination sources.

- Failure Mechanisms Associated with Submicron Metallic
  Interconnects in VLSI (R. F. W. Pease)

Scientific Objective

We are investigating the failure mechanisms associated with submicron (0.1 to 1 μm) metallic interconnects under conditions most likely to be encountered in submicron VLSI. Our initial area of investigation was electromigration in submicron aluminum conductors interconnecting semiconductor devices.

Progress

Failures caused by electromigration in metallic conductors have been investigated for more than 15 years [1,2,3]. As a result of this earlier work, pure aluminum is rarely used as an interconnect when dc current densities exceeding 10^4 A-cm^{-2} are liable to be encountered. Alloys of aluminum copper and silicon have proved to be more reliable, and dc current densities in the range of 10^5 A-cm^{-2} are now acceptable for most applications; however, the price paid is a reduction in electrical conductivity. When higher current densities are required, refractory metals can be used, but these also have their problems with an even greater increase in electrical resistivity.

When high speed is essential in VLSI, the simultaneous requirements for electromigration resistance and high electrical conductivity become particularly acute because the fastest circuits need large currents and negligible voltage drops.

There is considerable scatter in the results reported for mean times to failure of metallic conductors. Much of the work has focused on aluminum-alloy conduction of widths varying from 3 to 30 μm at elevated temperatures. Activation energies vary from 0.5 to 0.7 eV, and the dependence of mean time to failure on current density has been quoted from inverse linear to inverse cube and to even higher inverse powers. The distribution of failure times has been assumed to be lognormal, but we have observed that such an assumption is inconsistent with the published results.

There have been reports that, in lines of width below 2 μm (down to 0.8 μm), times to failure of E-gun deposited Al-Cu are often larger than expected [4]. This was attributed to the absence of grain boundaries along the direction of current flow and has been substantiated qualitatively for pure aluminum [5] with a similar structure.

Summary of Results

This project was initiated in June 1982. To date, the results include

- a literature search

- development of such techniques as lift-off to realize sub-micron metal lines

- an on-line computer pattern generator interfaced with a scanning electron microscope

- evaluation of wet chemical etches for decorating grain boundaries in evaporated pure aluminum

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B. Information Systems

1. Real-Time Statistical Data Processing

Principal Investigator: T. Kailath

Scientific Objectives

In the 1981 proposal, our goals were to study the potential applicability of a new class of algorithms developed by our group to specific problems encountered in radar and sonar signal processing.

The first area to be investigated was error analysis of our normalized lattice (or ladder) algorithms for autoregressive system identification, assuming rounding errors in the arithmetic. The second area was harmonic retrieval and, more specifically, the detection and estimation of sinusoidal signals in noise.

Progress

Error Analysis of Lattice Algorithms

While implementing an algorithm in special-purpose digital hardware or as a software routine, the effect of using finite register lengths must be taken into account. This effect manifests itself, especially in analog-to-digital conversion errors and in rounding errors caused by quantization of the result of such arithmetic operations as additions or multiplications.

The effects of quantizing the result of these arithmetic operations depend on whether the arithmetic is performed in fixed or floating point. In floating-point arithmetic, both addition and multiplication operations involve rounding; on the other hand, fixed-point addition does not increase the wordlength if the sum is guaranteed to be less than unity. We can expect, therefore, a better precision with fixed-point arithmetic if the quantities do not exceed unity in magnitude, which exactly occurs in the normalized lattice-filter algorithm.

The traditional approach to analyzing finite wordlength effects in digital filters is to model the roundoff errors as

uncorrelated zero-mean random variables and to compute the noise vari-
ance at the output of the filter contributed by the errors. In these
studies, the biases introduced in the desired output are negligible and,
as a result, our analysis is directed toward predicting the error
variance. Simulations of the fixed-point lattice-filter algorithms,
however, have demonstrated that the bias in the filter parameters (the
reflection coefficients) is much more predominant than are the variances
of the error in the estimates.

Harmonic Retrieval

The current approaches to the adaptive detection and
estimation of multiple sinusoids in noise are based on autoregressive
(AR) modeling of the observed process. These methods, often called
"maximum entropy," produce high-resolution spectral estimates when the
observed data closely fit an AR model; however, they yield biased esti-
mates when nonautoregressive data are involved as, for example, when
multiple sinusoids are observed in the presence of additive noise.
These methods are also off-line.

The adaptive line enhancer (ALE) introduced by Widrow is
an approximate transversal-filter on-line implementation of the AR spec-
tral estimator. In earlier work [2], we showed that an exact lattice-
form implementation of the ALE had substantially faster convergence
properties. Another approach, better suited for the harmonic retrieval
problem, was pioneered by Pisarenko [3] whereby the harmonic structure
of the signal was specifically exploited to obtain unbiased frequency
estimates even in the presence of additive white noise. This is a some-
what complicated off-line procedure, however, because it is based on the
computation of the smallest eigenvalue and the corresponding eigenvector
of the covariance matrix of the observed signal. A simpler on-line
implementation [4] was based on the stochastic approximation-gradient
algorithm.

Summary of Results

In our work on lattice algorithms, we have obtained a simplified theoretical expression for predicting the average bias in the estimated reflection-coefficient parameters. We have also derived a recursive relation for the average error (resulting from finite precision arithmetic) in the squared-error residual. This recursion illustrates how the error in one stage affects those in the succeeding stages. Simulations conducted to verify the theoretical model confirmed the predicted values. A paper on this topic has been completed [1] and was submitted to IEEE Transactions on Acoustics, Speech, and Signal Processing.

In the area of harmonic retrieval, we derived an approximate least-squares adaptive algorithm [5] which has a much faster initial convergence and resolves sinusoids more quickly than does Thompson's algorithm. In another direction, we have also extended our lattice-form implementation of the ALE to multiple sinusoids, and a paper [6] is being reviewed. In addition, we are exploring the properties of the maximum-entropy methods, and a paper comparing several of them for very short data records has been published.

References

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2. Signal-Processing Algorithms and Architectures

Principal Investigator: M. Morf

Scientific Objectives

The major goals of this research project are to

- further develop and unify fast algorithms and VLSI architectures for real-time signal processing, with emphasis on the study of parallelism, communication complexity, and programming environment

- study their applicability to specific problems in adaptive signal processing (for sonar, radar, and LIDAR), communication, and system identification

This research, begun several years ago under JSEP support, is continuing to attract considerable attention; it is now funded on a larger scale by other agencies, especially by DARPA for the VLSI aspects and by ONR for speech and signal processing.

Progress

Algorithms and VLSI Architectures

A major achievement during the last reporting period was the continuing development and unification of several new and previously developed ladder forms and array architectures for time-series modeling, signal processing, communication, and control. Our array and ladder algorithms enable solutions to many linear algebraic problems, including an exact least-squares solution to multichannel autoregressive and

moving-average modeling and a host of related topics; their simplicity and efficiency are a significant breakthrough. The theory and application of these ladder and lattice (two-dimensional array) forms are expected to have a strong impact on the general field of signal-processing and matrix computations. A tremendous amount of interest was generated by our presentations of the VLSI array architectures and recursive ladder forms, and the number of publications in this area is increasing at an exponential rate. Many practical applications exist wherein these techniques are being used or contemplated, such as communication (channel equalization, high-speed digital modems, data and speech encoding/ decoding), control, highly sensitive event detection (time of arrival, intruder detection, estimation of pitch or plosive sounds), high-resolution spectral estimation, channel equalization, adaptive signal processing (spectral line enhancement, noise cancellation, and inversion).

Another very significant development is our doubling, tree, and 2-D lattice algorithms for Toeplitz-related and general matrices. The need for inverting matrices appears in numerous problem areas. Our techniques considerably reduce the amount of computation required to invert large matrices. These developments are beginning to have an impact on real-time signal-processing tasks, such as array processing, beam forming, source location, image reconstruction, and distributed sensor networks.

Applications and Simulations of Fast Algorithms

Our current work in software development is aimed at establishing a program library that includes standard recursive identification methods, prewindowed ladder algorithms in both AR and ARMA forms, newly developed covariance and sliding-window ladder algorithms for fast parameter tracking, our speech-modeling system previously developed around the prewindowed ladder form, and several source-location programs. Event-detection algorithms that indicate when there is a sudden change in the underlying model of a plant or signal source evolved from earlier pitch-detection algorithms. All these algorithms

and associated programs are being examined for a variety of applications, both for software (possibly microcoded) and hardware (VLSI) implementations. From a software point of view, we are investigating the unification and standardization of program modules to implement the different algorithms. The hardware aspects are studied by determining how to compute elementary functions (add, multiply, divide, square-root, sine, cosine) and what are the ideal elementary operations and hardware modules [1]. CORDIC is becoming one of the most promising techniques; it can be viewed as a bilinear bang-bang control solution (or a series of reflections) to the problem of computing elementary functions and is ideally adapted to signal processing and to the class of algorithms we have been developing.

Summary of Results

The milestones accomplished during the reporting period are

- fast square-root ladder and 2-D lattice-form modeling algorithms (LADMO)

- fast doubling algorithms for large matrix decompositions and inversions

- VLSI chip designs for real-time digital signal processing (LADMOS)

- analysis of ARMA ladder forms, noise cancelling, and line enhancers

Many publications were concerned with the theory and application of ladder forms, and the number and diversity of research topics make it difficult to present a comprehensive summary. The first International Conference on Fast Algorithms was held in Aussois, France, during this past year.

References

1. H. M. Ahmed, "Signal Processing Algorithms and Architectures," Ph.D. dissertation, Department of Electrical Engineering, Stanford University, Stanford, Calif., Jun 1982.

2.   J.-M. Delosme, "Algorithms for Finite Shift-Rank Processes," Ph.D.
     dissertation, Department of Electrical Engineering, Stanford Uni-
     versity, Stanford, Calif., Aug 1982.

Annotated Bibliography of Our Recent Work under JSEP Support

FAST ALGORITHMS FOR FINITE SHIFT-RANK PROCESSES: A GEOMETRIC APPROACH,
J.-M. Delosme and M. Morf (invited), in the 1982 volume of the series
Mathematical Tools and Models for Control Systems Analysis and Signal
Processing, CNRS Editions, Paris, pp. 499-527.

Various algorithms acting on the covariance of processes with
finite shift-rank—fast Cholesky decomposition, fast inverse triangular
decomposition (or extended Levinson), and fast inversion via doubling—
are shown to be direct applications of some general updated formulas.
Their derivation involves the introduction of two random vectors ("gap"
variables) associated with any finite shift-rank process and systematic
use of simple arguments from linear least-squares estimation.

This work provides, for the first time, a unified and comprehensive
mathematical framework for the class of fast algorithms we have devel-
oped. It includes the new doubling (or function recursive) algorithms
that are most efficient for very large problems.

THE CONCURRENT SOLUTION OF LINEAR SYSTEMS OF EQUATIONS AND ITS RELATION-
SHIP TO FILTERING, J.-M. Delosme and M. Morf (invited), to be published
in Circuits, Systems and Signal Processing, Jan 1983.

The solution of many problems requires factoring or inverting some
matrix or solving a linear system of equations and, as a result, there
has always been a need for more efficient ways of performing these basic
operations of linear algebra. With the advent of very large scale inte-
gration, processing units and storage elements have become inexpensive
and this has modified the meaning of "efficiency." To achieve speed,
one now seeks algorithms with simple parallel implementation on an array
of processors. Simplicity implies that the processors (hardware) and
the data flow, memory management, and control (software) are not com-
plex. We have isolated the essential ingredients in the derivation of
such simple architectures—the choice of algorithms (of the elimination

type) and processors (of the CORDIC type), the proper selection between mappings of loops in time and space, the use of fundamental rules such as linear superposition, and flow reversal. Flow reversal is classical in the filtering area where simple rules help to determine by inspection the inverse of a filter if its graph representation is known. By developing a mapping between linear algebra algorithms and various filter structures, we are able to exploit the results obtained from the filtering field to develop elegant architectures for matrix computations.

The significance of this paper is its demonstration of the close relationship between matrix algebra, signal processing, and implementation (VLSI) architectures.

MATRIX DECOMPOSITIONS AND INVERSIONS VIA ELEMENTARY SIGNATURE-ORTHOGONAL TRANSFORMATIONS, M. Morf and J.-M. Delosme (invited), Proc. ISMM Symposium, San Francisco, Calif., May 1981.

A survey of matrix decomposition and inversion algorithms is presented. These algorithms can be applied to arbitrary matrices and, in contrast to standard algorithms, they relate to a class of fast algorithms for Toeplitz matrices and, more generally, for those with a small shift rank. The algorithms are based on orthogonal and signature-orthogonal transformations. Because such transformations can be decomposed into plane rotations and hyperbolic transformations, the CORDIC-like algorithms are perfect building blocks in implementing these procedures. All these features enable simple VLSI realizations.

This paper emphasizes the fundamental role played by indefinite signatures in matrix arithmetic and signal processing--a fact that, to date, has been largely ignored.

ENHANCEMENT OF SINUSOIDS IN COLORED NOISE AND THE WHITENING PERFORMANCE OF EXACT LEAST-SQUARES PREDICTORS, A. Nehorai and M. Morf, Trans. on Acoustics, Speech, and Signal Processing, ASSP-30, Jun 1982, pp. 353-363.

The extraction of sinusoids in white noise by means of least-squares predictors has attracted much attention in the past, principally in the context of the adaptive line enhancer (ALE); however, very few

results have been published for colored noise or for the whitening per-
formance of the predictors. We use a matrix formulation to derive the
optimal least-squares coefficients and frequency response of the D-step
predictor or ALE for sinusoids (real or complex) in additive colored
noise. New formulas have been obtained for the amplitude gain. In
lowpass background noise, the amplitude gain of the sinusoids becomes
essentially a monotonically increasing function of their frequency and a
decreasing function in highpass noise. For the whitening application,
output bounds on the signal-to-noise ratio were derived when the input
is a white signal plus sinusoidal interference. We also developed a
state-space model and stochastic interpretations of our analysis of the
D-step predictor to provide connections to other related areas. To en-
able filtering of nonstationary complex inputs, in addition to multi-
channel and multiexperiment data, our complex vector version of the
ladder algorithm can be used to implement the ALE, noise canceling, and
noise inversion for narrowband interference rejection.

EFFICIENT SOLUTION OF THE INVERSE LEVINSON PROBLEM IN THE MULTICHANNEL
CASE VIA THE LYAPUNOV EQUATION, M. T. Hadidi and M. Morf, Proc. 20th
IEEE Conf. on Decision and Control, 16-18 Dec 1981, pp. 1075-1076.

This paper introduces an efficient method for solving the discrete
Lyapunov equation when the system matrix is a block companion and for
solving the equivalent inverse Levinson problem in the multichannel case
[constructing ladder realizations for a given matrix autoregressive (AR)
model]. The condition for the existence of a unique solution is speci-
fied, and some of the results obtained for the scalar case are genera-
lized.

The significance of this paper is that it presents the solution to
a problem others have attempted to solve for more than ten years. This
solution demonstrates that our ladder-form parameterization is fundamen-
tal and becoming even more desirable.

A UNIFIED STOCHASTIC DESCRIPTION OF EFFICIENT ALGORITHMS FOR SECOND-ORDER PROCESSES, J.-M. Delosme and M. Morf, Proc. Fast Algorithms for Linear Dynamical Systems Workshop, Aussois, France, INRIA Publications, 21-25 Sep 1981, pp. 13.1-13.22.

This paper is a first version of "Fast Algorithms for Finite Shift-Rank Processes: A Geometric Approach." It presents a complete and unified view of algorithms for the modeling and whitening of stationary and nonstationary processes. These algorithms can be applied to speech analysis and synthesis, geophysical data processing, and antenna arrays.

RECURSIVE LEAST SQUARES LADDER ESTIMATION ALGORITHMS, D. T. L. Lee, M. Morf, and B. Friedlander, special joint issue of IEEE Trans. on Circuits and Systems, CAS-28, Jun 1981, pp. 467-481.

Recursive least-squares ladder-estimation algorithms have attracted much attention because of their excellent convergence behavior and fast parameter tracking compared to gradient-based algorithms. We have developed square-root normalized exact least-squares ladder-form algorithms that have fewer storage requirements and lower computational requirements than the unnormalized forms. This paper presents a Hilbert-space approach to the derivations of magnitude-normalized signal and gain recursions, and these normalized forms are expected to have even better numerical properties than the unnormalized versions; others, such as joint process estimators (adaptive line enhancer) and ARMA (pole-zero) models, are also presented as are their applications to fast (zero) startup equalizers, adaptive noise and echo cancellers, nongaussian event detectors, and inverse models for control problems.

DOUBLING ALGORITHMS FOR TOEPLITZ AND RELATED EQUATIONS, M. Morf, Proc. 1980 ICASSP, Denver, 9-11 Apr 1980, pp. 954-959.

A new class of doubling or halving algorithms for solving Toeplitz and related equations is presented in this paper. For scalar $n \times n$ Toeplitz matrices, they require $O(n \log^2 n)$ computations similar to the HGCD (half-greatest common divisor) algorithm of Gustavson and Yun. These new algorithms, however, are based on the "shift" or displacement rank $1 < r < n$, which is an index of how close a matrix is to being

Toeplitz, and requires less than $O(r^2 n \log^2 n)$ operations. The results obtained from a basic version of a doubling algorithm for such "r-Toeplitz matrices" are applied to related problems such as the inversion of banded, block, and Hankel matrices. This is the first paper on function-recursive algorithms for possibly nonstationary processes.

A NOVEL INNOVATIONS-BASED TIME-DOMAIN PITCH DETECTION, D. T. L. Lee and M. Morf, Proc. 1980 ICASSP, Denver, 9-11 Apr 1980, pp. 40-44.

This paper presents a novel innovations-based time-domain pitch-detection technique for speech-like signals, using one of our recursive least-squares ladder algorithms. It is based on the assumption that the speech-driving process consists of an approximately gaussian part (unvoiced) and a jump part (voiced). The pitch-pulse positions located by processing the innovations alone are not very accurate because of phase distortion, the effects of zeros, and inaccurate model-parameter estimates. In our ladder-form linear-prediction recursions, a log-likelihood function is recursively computed (on-line) for each speech sample. The derivative of this function becomes a sensitive measure of the extreme outlyers of the speech waveforms (samples that very likely do not fit gaussian statistics). When combined with the innovations of our ladder algorithms, good data are obtained by locating the pitch pulses by thresholding. This pitch-detection scheme has an advantage in that all the necessary variables are already computed in the ladder recursions and, as a result, it is suitable for fast on-line or even hardware (VLSI) implementations.

This paper demonstrates that ladder-form algorithms are well suited for nongaussian signal processing, particularly for event detection.

SCATTERING ARRAYS FOR MATRIX COMPUTATIONS, J.-M. Delosme and M. Morf, Proc. SPIE 25th Annual Intl. Tech. Symp., San Diego, 24-28 Aug 1981.

Several new mesh-connected multiprocessor architectures have been developed and adapted to execute highly parallel algorithms for matrix algebra and signal processing (such as triangular and eigen decomposition, inversion, and low-rank updating of general, Toeplitz-, and

Hankel-related matrices). Because these algorithms are based on scattering theory and information-preserving transformations, they exhibit local communication and simple control and memory management, which are ideal properties for VLSI implementation. The architectures are based on two-dimensional "scattering" arrays that can be folded into linear arrays either through time sharing or because of the simple computation wavefronts or the special structures (such as Toeplitz) of the matrices involved.

ALGORITHMS FOR FINITE SHIFT-RANK PROCESSES, J.-M. Delosme, TR No. M735-22, Information Systems Laboratory, Dept. of Electrical Engineering, Stanford University, Stanford, Calif., Sep 1982.

Several modeling and computational problems in linear least-squares estimation can be elegantly solved by exploiting the "shift" (or displacement) rank.

Ladder or lattice structures have become very popular in dynamic system identification and process modeling because they can increase the order of a model in a simple manner. Until now, the application of ladder structures has been limited to a smaller class of processes than that encompassed by the fixed-order structures. We have now extended the ladder forms to a wider class to yield a better approximation to arbitrary nonstationary processes.

The notion of shift rank, introduced a decade ago in the estimation field, is the key to such an extension. Processes modeled by constant-parameter traditional ladder and fixed-order structures are special finite shift-rank processes, and these algorithms have been generalized for the whitening and modeling of arbitrary finite shift-rank pocesses.

The main step in the derivation of these generalized ladder structures is the analysis of algorithms that factor the covariance of the process to be approximated by exploiting the shift-rank property. New minimal versions of these algorithms have been developed, and a specific derivation method is used for multiprocessor (VLSI) implementations of the ladder filters.

When only asymptotic results are required, the above methods appear to perform unnecessary computations. A typical example is the determination of the minimum-phase factor of a spectrum, based on the knowledge of the Fourier coefficients. It has been recognized, however, that the combination of a divide-and-conquer approach with the shift-rank property can be used for this calculation and will avoid the computation of superfluous quantities. The proposed algorithms were not practical, however, and we have derived some explicit updated formulas that improve the original procedures by several orders of magnitude and make this approach more useful.

SIGNAL-PROCESSING ALGORITHMS AND ARCHITECTURES, H. M. Ahmed, TR No. M735-21, Information Systems Laboratory, Dept. of Electrical Engineering, Stanford University, Stanford, Calif., Jun 1982.

The advent of very large scale integration (VLSI) has facilitated the construction of large systems on a single silicon chip. We have exploited this ability to design a powerful signal-processing chip capable of implementing such popular algorithms as the discrete Fourier transform, ladder filters, and associated matrix algebra.

The goal of this work was to map algorithms onto architectures by maintaining a close link with the theoretical basis of a certain signal-processing method. All of the algorithms considered can be cast into a mathematical framework involving generalized vector rotations. Unlike current signal-processing computers that emphasize rapid multiplication, the signal-processing architectures here are based, therefore, on the ability to perform vector rotations in generalized coordinate systems.

The CORDIC algorithm conveniently implements vector rotations with such simple components as adders, registers, and shifters. Unfortunately, however, throughput is severely compromised because of the need to perform special operations to account for the limited region of convergence and the spurious scale constants inherent in the method. New techniques resolve these problems, with no additional hardware and only a marginal speed penalty. Speed can be further enhanced through the use of a newly developed method known as hybrid CORDIC. In addition,

floating-point CORDIC (FLORDIC) algorithms are conceptually simpler than their fixed-point counterparts, and CORDIC can be connected to the convergence computation methods.

The architecture of a dual-CORDIC block chip can be applied to real-time speech analysis. The resulting chip has a higher throughput per area than do the conventional chips based on fast multiplications because of its close match to the algorithms.

Large mesh-connected processor architectures for matrix factorization were developed and were closely matched to the algorithms. Individual processing elements in the mesh were based on CORDIC operations--actually, on the signal-processing chip.

A new technique for signal detection in additive gaussian noise was also developed for ease of implementation. It is based on ladder filters and may be implemented using the same signal-processing chip.

3.   Signal Processing and Compression

Principal Investigators: R. M. Gray, M. E. Hellman, T. M.
         Cover, J. Gill

Scientific Objectives

The objective of this project is to study the basic limitations on the performance and efficiency of communication networks, including both multiuser and point-to-point systems. A parallel objective is to develop improved methods of signal processing for these systems from the structures used to verify the performance limitations. Attention will be directed toward the trade-offs between performance and complexity in signal-processing algorithms. Signal processing for data compression, improved signal-to-noise ratios, and privacy will be investigated.

Progress

Three projects (described below) focused on the computer-aided design of vector-quantization systems and tree-encoding data-compression

systems. These studies included extensive simulations, comparison to theoretical performance bounds from information theory, and comparison to traditional compression systems such as predictive quantizers and transform coders, with emphasis on performance and implementation complexity. Work has begun on other possible encoder structures that may reduce complexity with a tolerable loss of performance, particularly cascade codes and transform coders using vector quantization.

These projects have contributed to a better understanding of the merits of vector quantization and tree encoding for data-compression applications. We believe that the hybrid tree-coding system described below (and detailed in a paper appearing in the April 1982 issue of IEEE Trans. on Communications) is a promising alternative to the current systems of adaptive predictive quantization and subband coding with adaptive transform coding. The system is simpler, is automatically designed without recourse to the "bells and whistles" of much speech-coding work, and produces better quality at rates of 1/2 to 2 bits per sample.

a.   Discrete Logarithms (M. E. Hellman)

If α is a primitive element in $GF(q)$ which is the Galois field with q elements, the pair of inverse functions

$$Y = \alpha^X$$

and

$$X = \log_\alpha (Y)$$

are well defined over $GF(q)$ for $0 < X < (q - 2)$ and Y ranging over the nonzero field elements. The first is the discrete exponential function and the second is the discrete logarithm (or index) function.

This pair of inverse functions has long been of interest to a number of theorists and has recently gained practical importance because of its applications to cryptography [1] stemming from the apparent one-way nature of the discrete exponential function; it is easy to compute but appears difficult to invert. The difficulty in computing

discrete logarithms is critical to the security of several proposed cryptosystems and both conventional and public-key distribution systems.

Merkle [1] and Adleman [2] independently developed the fastest known algorithm for computing discrete logarithms for q = p (a prime). Adleman reported that its running time grows subexponentially in the length of the problem ℓ, where $\ell = m \ln (p)$. The bound obtained was roughly

$$\exp\left[\sqrt{k\ell \ln (\ell)}\right]$$

which grows slower than any exponential in ℓ but faster than any polynomial (for this algorithm, m = 1, and we believe that $k \approx 4$).

In the paper "Fast Computation of Discrete Logarithms" (submitted to IEEE Trans. on Information Theory), we discuss extensions of the algorithm to $q = p^m$ for certain values of p and m. Our method achieves subexponential asymptotic behavior when m grows and p is fixed. The method is of particular interest because $GF(2^m)$ is believed to have certain advantages for the public-key distribution system proposed by Diffie and Hellman [3,4].

To our knowledge, there is no subexponential solution for the discrete-logarithm problem when m and p are arbitrary, including, for example, logarithms in $GF(p^2)$; however, the discrete logarithm X in $GF(p^2)$ can be separated into two parts (x1 and x2) such that x = x1 + x2(p - 1), and it is then possible to obtain x1 in subexponential time because it can be written as some logarithm in GF(p). It is still a problem as to whether there is a fast algorithm for x2 or whether the index of elements in the group of order p + 1 can be computed rapidly. If such an algorithm exists, it may be possible to generalize it for larger extensions of GF(p).

Coin Flipping by Telephone

Two parties, A and B, may wish to agree on the result of a coin toss while they are conversing by telephone. A problem occurs if these two parties do not trust each other and do not have an

intermediary. In the paper "Coin Flipping by Telephone" (submitted to
IEEE Trans. on Information Theory), we presented a new protocol that
solves this problem and compared it to previous protocols.

Blum [5] introduced a protocol to solve this problem,
using Rabin's method of "oblivious transfer" [6]. This approach relies
on the difficulty of computing square-root modulo N, where N = pq is
the product of two unknown primes. If p and q are known, computing
square roots would be easy, and squaring modulo N would be a trapdoor
one-way function [3]. Shamir, Rivest, and Adleman [7] described how to
play "Mental Poker," and their scheme can be used for coin flipping.
They require trapdoor commutative one-way functions.

Our solution assumes the existence of two functions, f_h
and f_t (h for "head" and t for "tail"), having the following prop-
erties.

- Given y, it is computationally impossible to determine
  an x such that $y = f_h(x)$ or $y = f_t(x)$ (f_h and f_t
  are one-way functions).

- It is computationally impossible to find x and x' such
  that $f_h(x) = f_t(x')$.

- Both f_h and f_t have the same range, and each element
  in this range has the identical number of inverse images
  under both f_h and f_t.

After A and B have such a pair of functions, the coin-flipping pro-
tocol is straightforward.

- A selects some element x and sends either $y = f_h(x)$
  or $y = f_t(x)$ to B.

- B guesses which function (f_h or f_t) was used and
  sends his guess to A.

- A transmits x to B, and B computes $f_h(x)$ and
  $f_t(x)$ to confirm that A is playing fairly and to
  determine whether he won the toss by guessing correctly.

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Note that our method does not require that the one-way functions be commutative or have the trapdoor property and, in addition, the set of properties listed above can be relaxed considerably. For example, the one-way functions may be implemented by using the Data Encryption Standard [8]. We could choose $f_k(x) = DES(x, P_h)$, the encryption of the fixed plaintext P_h using the key x, and similarly for $f_t(x)$. Although the ranges of these two functions are not the same, they could serve well in our protocol.

We believe that the requirements of our method are not stringent and that a large number of one-way functions can be found to satisfy them. At present, we are able to provide only one example where the protocol can be proved secure, based on the assumption that discrete exponentiation [1] is a one-way function. Our protocol also differs from the "oblivious transfer" in that no party can force himself to lose or reduce his chances to win after f_h and f_t are determined.

Shift-Register Birthday Problem

We studied the expected number of bits in a random sequence before any 1-bit pattern repeats. This problem was motivated by a recently adopted National Standard of using the DES in an output-feedback mode to achieve a synchronous cipher. Our result indicates that the expected length of the sequence is on the order of $2^{1/2}$, and this exposes a weakness in the encryption method. A paper [9] on the solution of the probabilistic method has been accepted for publication in the Journal of Applied Probability.

Other Work

Two papers were accepted for publication in IEEE Trans. on Information Theory and will appear in the January 1983 issue. The first [10] is "On Secret Sharing Systems," and the second [11] is "The Largest Super-Increasing Subset of a Random Set" also presented at the IEEE International Symposium on Information Theory, Les Arcs, France, June 1982.

b.   A Theory of Multiple-User Communication (T. M. Cover)

We are developing a theory for the data compression of several sources. This problem is as yet unresolved although we have proposed a natural achievable region. Our general approach is to solve selected problems in the area of multiple-user communications in an attempt to piece them together to obtain a general theory of information flow in networks. We wish to bring the theory of delay under the information theoretic approach, and preliminary success in this direction has been achieved. We have also established that maximum-entropy distributions are the natural answers to probabilistic questions.

In the area of multiple-user communications, we have established

- a solution to the capacity region for degraded relay channels

- relativistic information flow (we have found that the same asymmetries in the flow of time appear in the flow of information; in the twin paradox, the traveling twin grows old less fast than does his stay-at-home brother and, in the information-transmission problem, the traveling transmitter requires more energy per bit sent than does his stay-at-home brother)

- an achievable rate region for the two-description problem

- a proof that the capacity of a multiple-access channel is not diminished when the senders are not synchronized

c.   Data-Compression Methods for Tree Data (J. Gill)

The problem of designing optimal encodings for arbitrary tree data has proven to be very difficult. As a result, we have concentrated on two areas. One is the use of ad-hoc methods whereby frequently occurring combinations of nodes are replaced by a single node whose descendants are all the descendants of the replaced nodes, and the other is the special case of linear data. We are experimenting with the compression of both sequential data files and interactive data communications.

Although the design of optimal codes for tree data remains open, we have developed an efficient encoding algorithm for any fixed-variable to fixed codebook. This algorithm operates in time proportional to the length of the tree data to be encoded and is based on dynamic programming. (The decoding algorithm is a very simple table-lookup procedure.)

In preliminary file-compression experiments, we have compressed text files to roughly 50 percent of their expanded size, and frequency measurements indicate that this compression can be improved to 35 percent. To be useful, however, file compression should occur automatically, without user intervention. We have studied several architectures that support data compression transparent to the files of several existing operating systems (UNIX, QUNIX, and CP/M). The major task in transparent compression is supporting random-access files. Our approach has been to store data in data blocks smaller than those used by the operating system, thereby storing more blocks in a fixed medium. Measurements and experiments to determine optimal block sizes are under way.

For interactive data communications, we must make use of adaptive-compression techniques and multiple codebooks. If we use alphabetic instead of Huffman codes, codebooks of n messages can be represented with 2n bits. In communications applications, n = 128; therefore, each codebook can be stored in 256 bits or 32 bytes. Compact storage of codebooks enables the practical use of first- or second-order Markov models of the data sequence (for example, 128 codebooks, one for each possible previous symbol, could be stored in only 4096 bytes). Efficient algorithms for encoding and decoding based on these codebooks are being designed.

Summary of Results

Three data-compression projects have been completed. The first considered the use of inverse-filter codebooks for both voice-coding (vocoder) and tree-encoding waveform compression systems for low- and medium-rate speech compression. The pitch-excited vocoder is a variation

of a speech-coding system based on vector quantization described in previous reports. The encoder selects a linear-predictive coder (LPC) inverse filter from a finite codebook that best "matches" an observed frame of sampled speech. This filter is then used to determine the voice and digitized pitch information. Unlike LPC systems, digitization is performed in a single step rather than in separate modeling and digitization steps. The tree-encoding system uses the filter selected as above to "color" a tree which is then searched for a minimum distortion path for the original sampled speech waveform. This system is a hybrid between the universal tree encoder developed at Stanford and previously reported and an adaptive predictive coder.

The second project (jointly supported by the Air Force Office of Scientific Research) focused on a generalization of a vector-quantizer algorithm used to design locally optimal (minimum average distortion) trellis-encoding data-compression systems, with emphasis on speech-waveform coding systems. This design algorithm is based on a training sequence of actual data from the source to be compressed to improve a given initial trellis decoder. An additional algorithm enables the automatic design "from scratch" of a trellis decoder for a given data source. A variation of the standard M-algorithm is employed as an encoder. The performance of the resulting codes was compared to those obtained by conventional techniques and, where possible, to theoretical bounds from information theory. Several coding structures were evaluated—straightforward waveform coding, residual excited linear-predictive coding systems, and a hybrid resembling an adaptive predictive quantizer. These structures were found to be superior to the comparable traditional systems in terms of complexity and performance.

Both of the above projects were extensions and completions of work previously described in JSEP reports. Papers were published in the April 1982 special issue of IEEE Trans. on Communications on bit-rate reduction and speech interpolation.

The third project was a study of full-search and tree-searched vector quantizers for Gauss-Markov sources. Extensive simulations were conducted to compare the locally optimal vector quantizers with

theoretical bounds to the more conventional predictive quantizers and transform coders for the Gauss-Markov source. In addition, the complexity of the various systems as determined by the number of arithmetic operations required for encoding was determined. A paper based on this work was published in the February 1982 issue of IEEE Trans. on Communications.

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